MAGNETIC [illegible]ALS INC.
A subsidiary of CONTROL DATA CORPORATION

ENGINEERING SPECIFICATION

NORMANDALE OPERATIONS

SPEC 64712400
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FLAT CABLE

INTERFACE SPECIFICATION

FOR

THE SMD, MMD, AND CMD FAMILIES

to be used by us. Someday?

RESPONSIBLE ORGANIZATION	ORIGINATOR	UNIT MANAGER	SECTION MANAGER	DEPARTMENT MANAGER
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NRMOPS PRODUCT MANAGEMENT			H Kriesbeck	
NRMOPS APPLICATIONS ENGINEERING				
NRMOPS DISK DRIVE DEVELOPMENT				
NRMOPS CIRCUIT DESIGN				
OKHMPI PRODUCT MANAGEMENT				
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OKHMPI DISK DRIVE DEVELOPMENT				
OKHMPI CIRCUIT DESIGN				
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7	X	X	X		X	
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ILLUSTRATIONS

FLAT CABLE INTERFACE SPECIFICATION FOR THE SMD, MMD, AND CMD FAMILIES

1.0 SCOPE

This document describes the Interface requirements of the Magnetic Peripherals, Inc. SMD, MMD and CMD type disk drives. For specific product characteristics see Table 1; for additional product detail reference SMD, MMD or CMD product specifications.

2.0 APPLICABLE DOCUMENTS

SPEC 64709300 - Product Specification Storage Module Drive (SMD)
SPEC 64709700 - Product Specification Mini-Module Drive (MMD)
SPEC 75888221 - Product Specification Cartridge Module Drive (CMD)

3.0 GENERAL DESCRIPTION

The Interface for all SMD, MMD and CMD devices use compatible line drivers and receivers. All Interface lines carry the same definition and timing conditions where commonality can be achieved. Some Interface lines have different timing requirements because of the basic product characteristics. The following Interface signals vary in the different products:

A. TAG 1
B. TAG 2
C. INDEX
D. SECTOR
E. SEEK ERROR
F. ON CYLINDER
G. SERVO CLOCK
H. SEEK END
I. SERVO OFFSET
J. WRITE PROTECTED

MODEL TYPE	PRODUCT TYPE	NO. HEADS	TRANSFER RATE	BYTES/ TRACK	BYTES/ CYLINDER	BYTES/ SPINDLE	CYLINDER/ DEVICE	FIXED HEAD CAPACITY	FIXED MEDIA CAPACITY	REMOVABLE MEDIA
9760/62	SHD	5 DATA 1 SERVO	9.677MHZ	20 160	100 800	41 428 800/ 82 958 400	411/823	NONE	NONE	ALL
9764/66	SHD	19 DATA 1 SERVO	9.677MHZ	20 160	383 040	157 429 440/ 315 241 920	411/823	NONE	NONE	ALL
9730-12/ 9730-24	MHD	2/4 DATA 1 SERVO	9.677MHZ	20 160	40 320/ 80 640	12 902 400/ 25 804 800	320	NONE	ALL	NONE
9730-12F/ 9730-24F	MHD	2/4 DATA 48 FIXED 1 SERVO	9.677MHZ	20 160	40 320/ 80 640 + FIXED HDS	12 902 400/ 25 804 800 PLUS 48 FIXED HEADS	320 +12 FIXED HD	967 680	ALL	NONE
9730-80	MHD	10 DATA 1 SERVO	9.677MHZ	20 160	100 800	82 958 400	823	NONE	ALL	NONE
9730-80F	MHD	10 DATA 1 SERVO 48 OR 96 FIXED	9.677MHZ	20 160	100 800 + FIXED HDS	82 958 400 PLUS 48 OR 96 FIXED HEADS	823 + (1) 10/20 (2) FIXED HEADS	967 680/ 1 935 360	ALL	NONE
9448-16/32	CHD	1/2 DATA 1/2 SERVO	9.677MHZ	20 160	20 160/ 40 320	16 289 280/ 32 578 560	823	NONE	0 16MB	16MB
9448-48/64	CHD	3/4 DATA 2 SERVO	9.677MHZ	20 160	60 480/ 80 640	48 867 840/ 65 157 120	823	NONE	32MB 48MB	16MB

(1) .96 MB FHT OPTION HAS 3 HEADS IN LAST CYLINDER

(2) 1.92 MB FHT OPTION HAS 1 HEAD IN LAST CYLINDER.

H367D

The data capacity specified is based on the number of eight-bit bytes that are recorded on a track. The unsectored capacity does not include an allowance for tolerance gaps.

TABLE 1. PRODUCT CHARACTERISTICS

4.0 ACCESSORIES

Accessory items required, but not furnished with the device are shown in the following tables:

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO.
"A" Cable (Controller to Device)	One per Device in star, one per multi-spindle installation in Daisy chain	2,3	775642XX
"A" Cable (Device to Device)	One less than total devices in the Daisy chain	1,2,3	775642XX
"B" Cable (Controller to Device)	One per Device	3	775643XX
Terminator	One per Device in star, one per multi-spindle installation in Daisy Chain	3	75841300

1. Multiple, number of cables required depends on number of units in daisy chain.
2. Last two digits denote length. (For cable length see Table 3.)
3. In systems using the dual channel operation, twice the number of cables and terminators are required.

The above accessories are required but not included with the units; they must be purchased separately.

TABLE 2. CABLES AND TERMINATORS

PART NO. TAB	CABLE LENGTH IN FEET									
	5	6	8	10	15	20	25	30	40	50
"A" Cable 775642XX	00	01	02	03	04	05	06	07	08	09
"B" Cable 775643XX	00	01	02	03	04	05	06	07	08	09

TABLE 3. I/O CABLE LENGTH AND TABS

DISK PACK DESCRIPTION	NOTE	PRODUCT DESIGNATION			
		9760	9762	9764/66	9448
Data Packs	2	9876 P/N 70439501	9877 P/N 70438001	9883-91 P/N 70430514	1204 P/N 76204000
CE Alignment Packs	1	876-51 P/N 70439001	877-51 P/N 70438700	883-51 P/N 70430003	TO BE SUPPLIED P/N 76204400

NOTES: 1. Quantity as required for regional maintenance.

2. At least one per spindle.

3. MMD type product is provided with non-removeable media.

TABLE 4. DISK PACKS (SMD/CMD)

	NOTE	PART NO.
TB3048 Field Exerciser	1,2,3	77449301
TB304C Field Exerciser	1,3	77449302
TB304_ Field Exerciser	1,2,4	TO BE SUPPLIED
Head Alignment Kit	1	77440500

NOTES: 1. Quantity as required for regional maintenance.
2. Includes head alignment capability.
3. Operates SMD, MMD but not CMD.
4. Operates SMD, MMD and CMD.

TABLE 5. MAINTENANCE EQUIPMENT

	QUANTITY REQUIRED	NOTE	PART NO.
Logic Plug	One per drive	1	943724XX
Single to Dual Channel Conversion Kit (9764/66)	One per drive		47205400
Single to Dual Channel Conversion Kit (9760/62)	One per drive		47205000
Single to Dual Channel Conversion Kit MMD	One per drive		To Be Supplied

NOTE: 1. Last two digits denote lens tab, one set (0 through 15) is provided with each SMD and CMD. MMD logic number selection is done by switch in logic chassis.
2. Dual channel not available in CMD.

TABLE 6. MISCELLANEOUS HARDWARE

5.0 INTERFACE

5.1 Interface Definition

The Standard "A" cable I/O is 60 pin configuration, the Standard "B" cable is 26 pin configuration.

All input and output signals are digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noisy electrical environment.

The "A" cable is a twisted-pair, flat cable. The "B" cable is a ribbon flat-cable with ground plane and drain wire. Twisted-pair and/or ground plane shielding is utilized to minimize cross-talk and reduce inductive coupling due to discharges, as well as control impedance variations regardless of cable lay.

5.1.1 Terminated, Balanced Transmission System

Transmitters and receivers of the industry standard types 75110A and 75108 or equivalent are used to provide a terminated, balanced transmission system (see Figure 1).

5.1.2 Line Transmitter Characteristics

The device controller line transmitters (Figure 2) shall be compatible with the MPI line receiver described in 5.1.3.

1. Output Signal Levels

   Control Signals - See Figure 2
   Data Signals - See Figure 1.

2. Output Line Polarity

   Control Signals - The MPI transmitter (Figure 2) shall be connected to the I/O line such that the output, labeled Z, shall correspond with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B, except for the unit selected line which is connected in the opposite manner.

   When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver, except for the unit selected line where a logical 1 into the transmitter produces a logical 0 out of the receiver.

5.1.3 Input Amplifier (Receiver) Characteristics

The Device Controller input amplifier (Figure 3) is compatible with the MPI transmitter described in 5.1.2.

1. Receiver Propagation Delay

The receiver propagation delay shall typically be 17 ns in the direction of the logical 1, and 17 ns in the direction of the logical 0.

2. Receiver Input Polarity

Control Signals - The input (labeled "B") of the receiver (Figure 3) is connected to the lowest numbered pin of the pair in the cable and in turn connected to the transmitter pin labeled Z.

Data Signals - See Figure 1.

5.1.4 Terminator

1. "A" Cable

A terminator resistance as shown in Figures 2 and 3 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly which must be ordered separately.

A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect line. See Paragraph 5.2.2-7. No termination resistance is used on the Power Sequence lines in the "A" cable.

2. "B" Cable

A termination resistance as shown in Figure 1 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card.

5.1.5 I/O Cables (See Figures 15A, 15B, 15C, 15D and 16)

5.1.5.1 "A" Cable

ITEM	DESCRIPTION	MPI P/N	BERG P/N	P/N SPECTRA-STRIP
1	Connector (60 Pos)	94361115	66043-007	
1.a	Contact, Insert	94245603	48048	-----
2	Flat Cable (twisted-pair), 30 pair, 28 AWG	95043902		3CT-6028-78-05-100

5.1.5.2 "A" Cable Mating Receptacle on Unit or Controller

ITEM	DESCRIPTION	MPI P/N	AMP P/N
1.a	60 pin, right angle header	94369804	3-86479-4
1.b	60 pin, vertical header	94385129	3-87227-0

5.1.5.3 "B" Cable

ITEM	DESCRIPTION	MPI P/N	AMP P/N
1.a	Connector (26 pos.)	65853402	3399-3000
.b	Connector Pull Tab	92004801	3490-2
2.	Flat Cable (26 pos.) with ground plane and drain wire.	95028509	3476-26

5.1.5.4 "B" Cable Mating Receptacle on Unit or Controller

ITEM	DESCRIPTION	MPI P/N	AMP P/N
1.a	26 pin, right angle header	94369802	1-86479-0
1.b	26 pin, vertical header	94385106	1-87227-3

5.1.6 I/O Cable Characteristics

"A" Cable

Type: 30 twisted pair, flat-cable
Twists per inch: 2
Impedance: 100 ±10 ohms
Wire size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft
Maximum cable length: 100 ft cumulative
Voltage Rating: 300 V rms

"B" Cable (with ground plane)

Type: 26 conductor, flat cable with ground plane and drain wire
Impedance: 130 ±15 ohms (3M P/N 3476-26)
Wire size: No. 28 AWG, 7 strands
Propagation velocity: 1.65 ns/ft (nominal)
Maximum cable length: 50 ft
Voltage Rating: 300 V rms

5.2 Signal Lines

5.2.1 Address and Control Tag Functions (received by the unit)

Address and control functions are transferred on 10 lines. The significance of the information on these lines is indicated by one of three tag lines (see Figures 4, 5A, 5B and 6).

5.2.1.1 Cylinder Address (Tag 1)

A. SMD and MMD Moving Head

Ten bus lines (Tag 1) are used to carry the cylinder address to the device. Since the device is a direct addressing device, the Controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure 7A). The unit must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

B. CMD

With the CMD, Tag 2 must precede Tag 1 when a volume change is made, that is, switching from fixed media to removable or removable to fixed. The correct servo head will be enabled at the trailing edge of Tag 1 (see Figure 7B).

C. MMD Fixed Head Tag and Bus

Transfer of cylinder and head address information is controlled by the same timing requirements as the moving head sequence which is defined in Figure 7A. Because no positioner move is involved and it would be expected that a head select would immediately follow a cylinder select, the minimum Tag/Bus timing is as shown in Figure 7C.

The fixed heads may be used to either read or write data while the moveable head positioner is in motion. The normal sequence of events would occur in the following order:

1. The controller issues a cylinder select with the desired moveable head cylinder location on the buss. "On Cylinder" and "Seek End" will drop.

2. The controller accesses the desired fixed head location with the appropriate cylinder select and head select signals.

3. Conforming to the specified times for head select to read or write, the controller can read or write on the fixed head memory. The absence of "On Cylinder" and "Seek End" will not cause a "fault" in the unit when reading or writing on the fixed head shoe.

4. At the completion of the seek by the moveable head positioner, "On Cylinder" and "Seek End" will become true.

5. When the read or write operation is complete on the fixed head, the controller may readdress the moveable heads by sending the appropriate cylinder select (zero track seek) and head select signals. The cylinder select command is required in order to clear the fixed head mode.

5.2.1.2 Head Select (Tag 2)

SMD - This signal is the head address that will be selected by bits present on the bus lines when Tag 2 is true. The Logical/Physical Addressing relationship for the SMD is in Table 7 summarized below:

MEDIA DATA	SMD 40/80/MB	SMD 150/300 MB
Data Surfaces/Device	5	19
Moveable Heads/Surface	1	1
Fixed Heads/Device	0	0
Moveable Cylinders/Device	411/823	411/823
Fixed Cylinders/Device	0	0
Moveable Heads/Logical Cylinder	5	19
Fixed Heads/Logical Cylinder	0	0
Moveable Cylinder Addresses	0-410/0-822	0-410/0-822
Fixed Cylinder Addresses	-	-

TABLE 7 LOGICAL/PHYSICAL ADDRESSING SMD

M368A

MMD - This signal is the head address that will be selected by bits present as the bus lines when Tag 2 is true.

With the fixed head option incorporated in the MMD, the 48/96 physical fixed heads are addressed by the controller as logical cylinders. This addressing scheme allows maximum interface commonality with the moving head storage of the MMD and also with the SMD family. The logical/physical addressing relationship for these devices is summarized in Table 8 below:

MEDIA DATA	MMD 12 MB	MMD 24 MB	MMD 80 MB	
DATA SURFACES/DEVICE	1	2	5	
MOVEABLE HEADS/SURFACE	2	2	2	
FIXED HEADS/DEVICE	48	48	48/96	
MOVEABLE CYLINDERS/DEVICE	320	320	823	
FIXED CYLINDERS/DEVICE	12	12	10/20	
MOVEABLE HEADS/LOGICAL CYLINDER	2	4	5	
FIXED HEADS/LOGICAL CYLINDER	4	4	5 (1) (2)	
MOVEABLE CYLINDER ADDRESSES	0-319	0-319	0-822	
FIXED CYLINDER ADDRESSES	896/907	896/907	896/905/915	

(1) .96 MB FIXED HEAD OPTION HAS 3 ADDRESSABLE HEADS IN CYLINDER 905.

(2) 1.92 MB FIXED HEAD OPTION HAS 1 ADDRESSABLE HEADS IN CYLINDER 915.

TABLE 8. LOGICAL/PHYSICAL ADDRESSING MMD

M369C

CMD - In the CMD this tag transmits head and volume address bits on the bus lines to the device (Figure 5B). This command must be followed by a valid seek command, (Tag 1) if the selected volume is different than the previously selected volume, since a volume change is not executed until the next valid cylinder address code; see table.

2^{9}*	2^{2}	2^{1}	2^{0}	BUS BITS
0	0	0	0	HD No. 0 REM
1	0	0	1	HD No. 1 FXD
1	0	1	0	HD No. 2 FXD
1	0	0	0	HD No. 0 FXD
1	0	1	1	HD No. 3 FXD
1	1	0	0	HD No. 4 FXD

TAG 2 BUS DECODE FOR CMD

* This bit is volume address which is stored in a bistable within the 9448 drive. The stored volume address and "TAG 1" result in a volume select if the cylinder address is valid.

The Logical/Physical Addressing relationship for the CMD is summarized below:

MEDIA DATA	CMD 16 MB	CMD 32 MB	CMD 48 MB	CMD 64 MB				
Data Surfaces/Device	1	2	3	4				
Moveable Heads/Surface	1	1	1	1				
Fixed Heads/Device	0	0	0	0				
Moveable Cylinders/Device	823	823	823	823				
Fixed Cylinders/Device	0	0	0	0				
Moveable Heads/Logical Cylinder	1	2	3	4				
Fixed Heads/Logical Cylinder	0	0	0	0				
Moveable Cylinder Addresses	0-822	0-822	0-822	0-822				
Fixed Cylinder Addresses	-	-	-	-				

M3708

LOGICAL/PHYSICAL ADDRESSING CMD

5.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation.

1. Write Gate (Bit 0)

   The Write Gate line enables the write driver (Figure 5A and 5B). See Figures 8A and 8B for typical Write Gate Timing requirements.

2. Read Gate (Bit 1)

   Enabling of the Read Gate (Figure 5A and 5B) enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern. (See Figures 8A and 8B for typical Read Gate Timing.)

3. Servo Offset Plus (Bit 2)

   SMD/CMD - When this signal is true, the actuator is offset from the nominal On Cylinder position towards the spindle. (See Figure 7A/7B for timing.) When dropping Offset Plus, a 4 ms delay is required before a Read or Write is initiated. When servo is in an offset mode, no write operation should be attempted.

   MMD - When this signal is true, no physical movement of the heads is performed in the drive, used only to meet timing requirements of SMD Drive Family. (See Figure 7A for timing.)

   CMD only - If Write Gate is brought up when offset is active, the Fault line will become true. Fault will go false when offset is cleared or Write Gate is dropped.

4. Servo Offset Minus (Bit 3)

   SMD/CMD - When this signal is true, the actuator is offset from the nominal On Cylinder position away from the spindle. (See Figure 7A/7B for timing.) When dropping Offset Minus, a 4 ms delay is required before a Read or Write is initiated. When servo is in an offset mode, no write operation should be attempted.

   MMD - When this signal is true, no physical movement of the heads is performed in the drive. Used only to meet timing requirements of SMD Drive Family. (See Figure 7A for timing.)

   CMD only - If Write Gate is brought up when offset is active, the Fault line will become true. Fault will go false when offset is cleared or Write Gate is dropped.

5. Fault Clear (Bit 4)

A pulse, 100 ns minimum, sent to the Device will clear the fault flip-flop if the fault condition no longer exists.

6. AM Enable (Bit 5) (See Note)

The AM (Address Mark) Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks (Figure 8A). When AM Enable is true while Write Gate is true, the writer stops toggling and erases the data, creating an Address Mark. Write Fault detection in the unit is inhibited during writing of an Address Mark.

When AM Enable is true while Read Gate is true, an analog voltage comparator detects the absence of read signal. If the duration of the erased area is greater than 16 bits, an Address Mark Found signal will be issued.

NOTE: If Address Mark is not used, Bit 5 must be held to a logical 0 during Control Select functions.

7. RTZ (Bit 6)

A pulse, 250 ns minimum, 1.0 ms maximum, sent to the device will cause the actuator to seek track 0, reset the Head Register, select the cartridge volume (CMD only), and clear the Seek Error flip flop.

This seek is significantly longer than a normal seek to track 0, and should only be used for recalibration, not data acquisition.

8. Data Strobe Early (Bit 7)

When this line is true, the Device PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

9. Data Strobe Late (Bit 8)

When this line is true, the Device PLO Data Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

NOTE: The Data Strobe signals are intended to be an aid in recovering marginal data. The data strobe position returns to nominal when the respective signals go false.

10. Release (Bit 9) (Dual Channel Only)

Enabling this line will release Channel Reserve and Channel Priority Select Reserve in the device, making alternate channel access possible after selection by the other channel ceases. If the unit is desired to function with "Reserved Timer" feature, release will occur 500 ms (nominal) following the deselection of the device. If a longer or shorter time is desired, the timer may be customer altered by changing a resistor and capacitor to obtain delays from 500 ns to 10 seconds. Enabling Release will always clear Reserve and allow alternate channel access independent of the Reserve Timer feature. The Reserve Timer is enabled by means of a switch in the logic chassis. Inhibiting the Reserve Timer causes the device to stay Reserved until specifically released by the operating channel. A unit is Reserved immediately upon selection, but may be released any time after 500 ns following selection. By means of a switch in the logic chassis, it is also possible to absolutely reserve a device to one or the other channels.

5.2.1.4 Unit Select

Priority Select (Bit 9) (Dual Channel Only)

When this line is true, the unit will be unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the Priority Select function has been performed the respective channel has exclusive access to the drive. The opposite channel can gain access only after a release function has been performed on the selected channel (see 5.2.1.3-10). For timing see Figure 9. Following a priority select on one channel all interface signals are inhibited on the opposite channel including "Unit Selected" and Busy".

5.2.2 Individual Lines

1. Sector Mark

A. SMD/MMD

The sector mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 10). The number of sectors per revolution is switch selectable and is determined by counting dibits/sector clocks. The switches are located on a card within the logic chassis. Each switch represents a fixed number of dibits/sector clocks when closed.

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
No. of dibits/ sector clocks:	1	2	4	8	16	32	64	128	256	512	1024	2048

To calculate the proper switch positions for the number of sectors desired, use the following formula:

$$\frac{\text{Dibits or Sector Clocks/Revolution}}{\text{No. Sectors}} = \text{Dibit or Sector Clock Count/Sector}$$

Example for 8 sectors: $\frac{13\,440}{8} = 1680$

close switch	10	= 1024
	9	= 512
	7	= 128
	3	= 8
	2	= 4
	1	= 2
One dibit or sector clock for SM Counter Reset	0	= 1
		1680 dibits or sector clocks/sector

Each dibit or sector clock (806 kHz clock) is equivalent to 12 data bits.

B. CMD

The sector pulse is derived from the servo track. Timing integrity is retained when Ready is active, and throughout seek operations in which no volume change is effected. There are 63 sector pulses available per revolution (see Figure 17). When combined with index in the controller, this divides the tracks into 64 even length sectors. Other sector counts are available by changing the sector switches whose binary weight indicates the number of sectors desired.

NOTE: The sector pulses will be inhibited upon receiving the Cylinder Tag associated with a volume change until the detection of the first index of the new volume (see Figure 17).

NOTE: Not all sector counts are even length. For example, a 50 sector option would allow 50 even length sectors with an odd length sector at the end. The following even length sector counts are available: 4, 5, 6, 7, 8, 10, 12, 14, 15, 16, 20, 21, 24, 28, 30, 32, 35, 40, 42, 48, 56, 60, 64, 70, 80, 84, 96, 105, 112, 120, and 128.

2. Fault

When this line is true, a fault condition exists in the device. The following types of faults may be detected by the device: DC Voltage Fault, Head Select Fault, Write Fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition will immediately inhibit the writer to prevent data destruction. The DC Voltage Fault indicates a below normal voltage from the positive or negative power supplies. The Head Select Fault indicates that more than one head is selected. The Write Fault indicates low for the absence of} write current or the absence of write data.

This line may be cleared by Control Select, or Fault Clear on the Operator Panel, or Master Fault Clear on the Fault card {providing the fault no longer exists}. Faults are also stored in individual flip flops as a maintenance aid, and may be cleared only by powering down dc power or clearing the fault by means of the switch on the fault card. The stored maintenance aid has no effect on unit operation.

NOTE: CMD - For fault summary, see paragraph 7.2 in Product SPEC.

3. Seek Error

When this line is true, a Seek Error has occurred. The error may only be cleared by performing an RTZ. This signal indicates that the unit was unable to complete a move within 500 ms, {except MMD} or that the carriage has moved to a position outside the recording field or received an illegal track address. A Return-to-Zero Seek Command will clear the Seek Error condition, return the heads to cylinder zero, and enable an On Cylinder signal to the Controller.

SMD - If an address greater than 823 tracks {411 tracks for 9760/9764} is addressed, the Seek Error signal will go true within 100 ns of the Cylinder Select Tag, and the carriage movement is inhibited to one track or less.

MMD - 12 and 24 megabyte versions will not decode a Seek Error for an illegal track address until the positioner move the heads into a guard band area. This requires approximately 65 ms under worst case conditions. There is no seek error status for cylinders beyond the designated fixed head cylinders.

The 80 megabyte version will decode a Seek Error for an illegal track address of 823 to 895 for the moving head portion. A seek error will also be decode at cylinder 916 and above for fixed heads. The device will not decode a Seek Error in units without fixed heads or units with only one fixed head shoe {48 heads} if the designated fixed head cylinders are addressed.

CMD - If an address greater than 823 tracks is addressed, the Seek Error signal will go true within150 µs maximum of the Cylinder Select Tag. Carriage movement is inhibited.

4. On Cylinder

This status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms (nominal) for all devices.

SMD - For a zero track seek, On Cylinder drops for 30 µs (nominal) (see Figure 7A for timing).

MMD - For a zero track seek, On Cylinder drops for 30 µs (nominal). For a seek to fixed head cylinders, On Cylinder drops for 5 µs maximum (see Figures 7A and 7C for Timing).

CMD - For a zero track seek on the same volume, On Cylinder drops for 150 µs maximum. For a zero track seek with a volume change, On Cylinder drop for 4 ms maximum (see Figure 7B for Timing).

5. Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 2.5 µs (see Figure 10). Timing integrity is retained throughout seek operations for all devices.

CMD - Index will become invalid when a volume change is made. Index will remain invalid until the new servo head is selected and Index is properly decoded on the new volume. Index signal to the controller is gated off during a volume change. If volume switch occurs within an Index Time, the pulse will not be gated off, it will be allowed its full time out. Upon changing volumes the first index from the newly addressed volume may occur in an interval of from 250 µs to 17.3 ms after the volume change is initiated.

6. Unit Ready

When true, and the device is selected, this line indicates that the device is up to speed. The heads are positioned over the recording tracks, and no fault condition exists within the device.

7. Open Cable Detector

The open cable detect circuit (see Figure 3) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation on the drive before the controller in Ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 ohm termination resistance to ground should be used at the controller end.

8. Unit Select Tag

This signal gates the desired logic number into the logic number compare circuit. The unit will be selected internally 600 ns (maximum) after leading edge of this signal. For timing see Figure 11. Note that this function must be edge triggered.

In Dual-Channel units, Unit Select Tag also forces the device to be reserved to that channel, providing selection occurs. The reserve will not be cancelled unless by release command, Reserve Timer or dc power-down/power-up. If Bus Bit 9 and the desired logic number is present with Unit Select Tag, a Priority Select will be performed, refer to paragraph 5.2.1.4. The unit will be selected internally 600 ns (maximum) after leading edge of Unit Select Tag. For timing see Figure 11. If both controllers request access simultaneously, Channel A will be granted priority.

9. Unit Select (2^0, 2^1, 2^2 and 2^3)

These four lines are binary coded to select the logical number of 1 of 16 devices. The unit number (0 through 15) is selectable by means of switches located on a card in the logic chassis (MMD) or on a logic plug on the unit's operator panel (SMD and CMD).

10. Address Mark Found

Address Mark Found is a pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

The controller must drop the Address Mark Enable line (Bit 5) upon receiving Address Mark Found (AMF) and valid data will be presented on the I/O lines following the AMF pulse. Upon sensing the dropping of Address Mark Enable line, the Address Mark Found pulse will be reset within 8.0 µs maximum (see Figure 8).

NOTE: Under certain conditions it is possible that the MMD could issue a false Address Mark Found signal during an address mark search operation. This would occur if a media flaw existed which simulated the electrical characteristics of an address mark (at least 16 missing transitions followed by a zero).

It is recommended provisions be made in system hardware or software to allow recovery from, or avoid the possibility of detecting false AMF signals.

11. Unit Selected

When the four Unit Select bit lines compare with the settings of the Unit Select switches in the logic chassis, and when the leading edge of Unit Select tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable (see Figure 11). Multiple Unit Selected responses on a daisy-chain system indicate duplicate switch settings have been used.

12. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a LED located on logic cards in MMD and on the operator panel in SMD and CMD, and sends a Write Protected signal to the controller. Attempting to write while protected will cause a fault to be issued. The Write Protect function is enabled by a switch located on a card in the logic chassis on the MMD and by a switch or switches on the operator panel on the SMD and CMD.

CMD only - When this line is true, it indicates that the 9448 is write protected. This signal will occur during maintenance when Head Alignment is being performed, during fault conditions that inhibit the writer, or when write protection is desired on the 9448 by depressing either of the PROTECT switches. If Write Gate becomes true when the drive is write protected on the selected volume, then the Fault Line will become true. The write protected condition can be cleared by depressing the appropriate PROTECT switch or by clearing the causing condition as appropriate.

13. Seek End

Seek End is the combination of ON CYLINDER or SEEK ERROR indicating that a seek operation has terminated.

SMD - For a zero track seek, Seek End drops for 30 µs nominal (see Figure 7A for Timing).

MMD - For a zero track seek, Seek End drops for 30 µs nominal. For a seek to fixed head cylinders, Seek End drops for 5 µs maximum (see Figures 7A and 7C for Timing).

CMD - For a zero track seek on the same volume, Seek End drops for 150 µs nominal. For a zero track seek with a volume change, Seek End drops for 4 ms maximum (see Figure 7B for Timing). If a cylinder address greater than 822 has been selected (illegal cylinder address), Seek End will go false for approximately 150 µs.

In Dual Channel Drives the Seek End Signal sent to the unselected channel will normally be a constant one. However, if while the Drive is selected on a channel, and the opposite channel receives a select, this action will be noted by circuitry within the Drive. Then, when the selected channels Select and Reserve Latches are cleared, the Seek End signal sent to the waiting channel will go to a zero for 30 µs.

14. Power Sequencing (see Figures 12A, 12B, 12C and 12D)

Power Sequencing requires ac power on, START switch on, and REMOTE START switch (switch selectable in device) in the Remote position. Applying ground to the Pick and Hold lines will cause the first device in sequence to power up. Once this device is up to speed, the Pick signal is transferred to the next active device and repeated until all active devices are powered up. Individual devices may be started and stopped once power sequencing is completed.

A power failure necessitates a new power up sequence.

When in Local Start mode, each device is independently operated by its respective START switch.

In the Remote Mode, a Pick or Hold is considered to be present from the Controller when a ground is present on "A" cable Pin 29 for Pick and Pin 59 for Hold.

15. Busy (Dual Channel Only)

If the device is already reserved and/or selected, a Busy signal will be issued to the "A" cable and unit selected will be issued on the "B" cable to the channel attempting the select. This busy signal will be issued from the device at its I/O connector within 600 ns following the selection attempt, and will remain at this status until Unit Select tag is dropped or the unit is no longer busy. Unit Selected should be used to enable Busy in the Controller (see Figure 11 for Timing).

NOTE: The CMD has no Dual Channel option.

5.2.3 Data and Clock Lines (Figure 13)

1. Write Data

This line carries data which is to be recorded on the disk pack.

2. Servo Clock

The servo clock is a phase-locked 9.677 MHz clock generated from the servo track quadbits on the MMD, and dibits on the SMD and CMD. This phase-locked clock (Figure 13) is used to generate write data. Servo clock is available at all times (not gated with Unit Select). For CMD, servo clock is rephased at a volume change (see Figure 17).

3. Read Data

This line transmits the recovered data in the NRZ form (see Figure 13) data.

4. Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 13. This signal is transmitted continuously, and is in phase sync within 9 µs after Read Gate.

5. Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ data as illustrated in Figure 13. The Write Clock is the Servo Clock retransmitted to the device during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Enable.

5.3 Data Format and Data Control Timing

The Record Format on the disk is under control of the controller. The index and sector pulses are available for use by the controller to indicate the beginning of a track or sector. Suggested formats for fixed and variable sector data records are shown in Figures 14A and 14B.

Some hardware-oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

1. Read Initialization Time

   Between the deselection of one head and the selection of another head, there is a 5.0 µs delay within the device due to circuit characteristics. The time from the initiation of a head change until data can be read with a selected head without error, is 24.0 µs, maximum (5.0 µs for head selection, and 10 µs for read amplifier stabilization and 9.0 µs for phase lock synchronization).

2. Write-To-Read Recovery Time

   Assuming head selection is stabilized, the time lapse before read gate can be enabled after switching the write gate off is 10 µs, minimum.

3. Read-To-Write Recovery Time

   Assuming head selection is stabilized, the time lapse from dropping read gate to enabling write gate shall be 0.3 µs, minimum (see Figures 8A and 8B).

4. Beginning-of-Record Tolerance (See notes on Figures 14A and 14B)

   This tolerance must be provided to allow for worst case conditions of head skew and circuit tolerances.

   This gap must be written with a minimum of 16 bytes of zeros.

5. Read PLO Synchronization

   The synchronization time needed to allow the phase-locked oscillator to synchronize is 9 µs of zeros.

6. Sync Pattern

   The Sync Pattern consists of "one" bits indicating the beginning of the address or data area (one "one" bit is the minimum required).

7. Write Driver Turn On

The Write Driver Turn On time is about 0.8 µs or one byte. This time has to be accounted for in order to know where possible splice areas are located.

8. End-of-Record Tolerance (See notes on Figures 14A and 14B)

This tolerance is an eight byte pad of zeros which eliminates the possibility of destroying the end of a record written with a late displacement head.

5.3.1 Write Format Procedure

Provisions must be made within the Controller to format the disk. The following procedure is recommended for fixed sector formats:

PROCEDURE

1. Select desired unit, cylinder, volume (CMD only), head and sector.

2. The Controller must provide a 5 µs minimum delay between selecting a head and initiating a search for leading edge of sector. This delay will ensure that the unit will be ready to write when the sector leading edge is detected.

3. Search for leading edge of desired sector.

4. Detect leading edge of selected sector.

5. Immediately bring up Write Gate and start writing zeros.

6. Write all zeros for head scatter and PL0 sync areas (27 bytes).

7. Write a sync pattern, the address, and the address checkword.

8. Write all zeros for write splice gap and PL0 sync field (12 bytes).

9. Write a sync pattern, the data field, the two byte data field checkword, and the one byte pad. The data field should preferably be a worst case pattern.

10. The end tolerance gap is the only part of the format where there may be erased areas with no write data. If erased areas occur in Gap 2 there may be problems in recovering the data following this gap. It is preferable to write zeros to the next sector pulse.

11. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate may be left on. In this case, the Controller should write all zeros in the tolerance gap.

5.3.2 Control Timing (Figure 8A or 8B)

1. Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase locked oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ±4 clock counts after the leading edge of index or sector.

The sync pattern search may begin 88 servo clock counts after the leading edge of Read Gate, or after the trailing edge of Address Mark Found.

Head switching and read amplifier stabilization (see Figure 8A or 8B) shows the latest acceptable time at which a head can be selected in order to read the next successive sector (with the format described in 5.3).

Data I/O lines may not have valid data until 9 µs from leading edge of Read Gate, due to phase lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up.

2. Write Data Field

The control line associated with a Write operation is Write Gate.

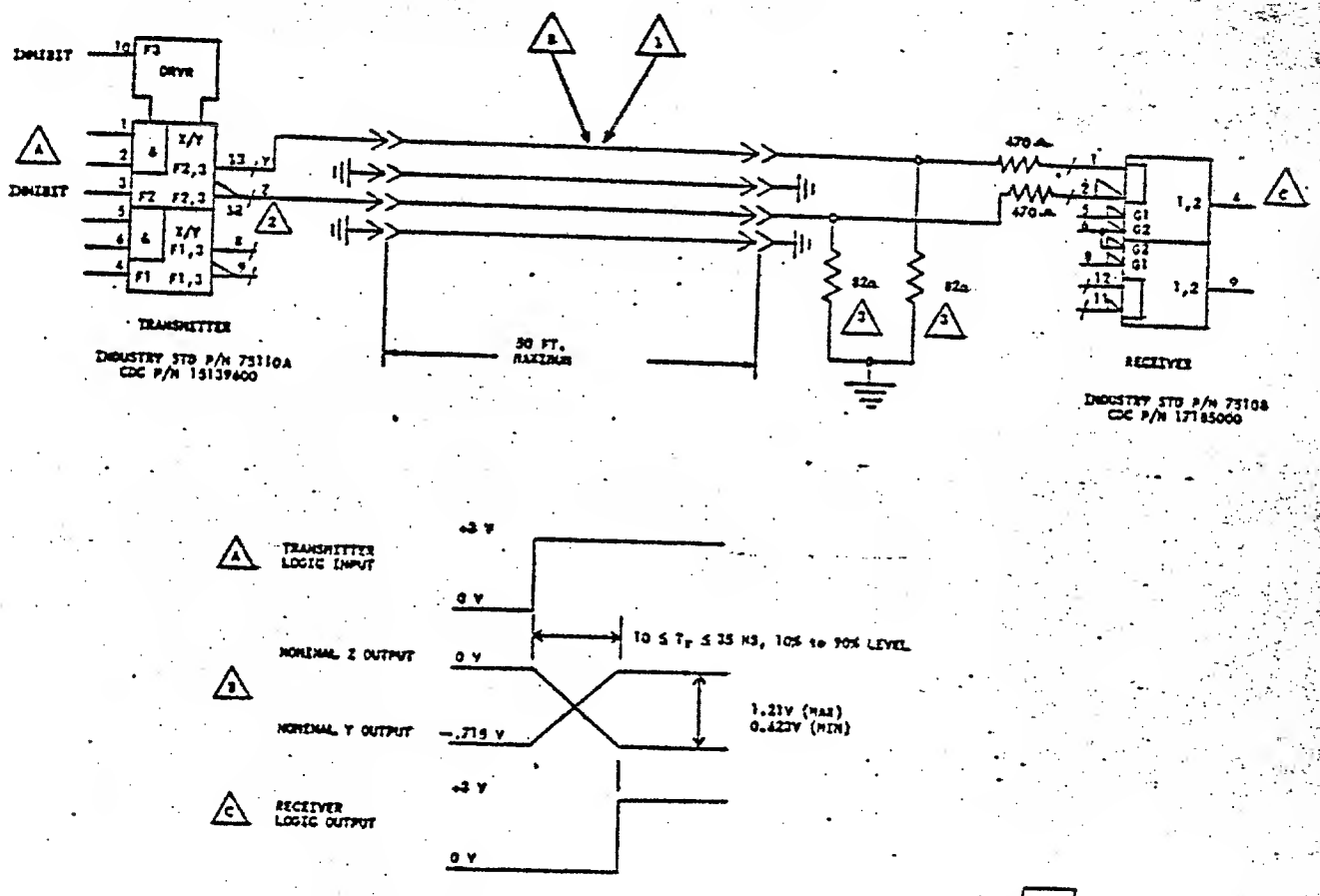
The sector address must always be read and verified prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the PLO sync field and sync pattern.

The Controller must provide a three bit internal delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 8A or 8B). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

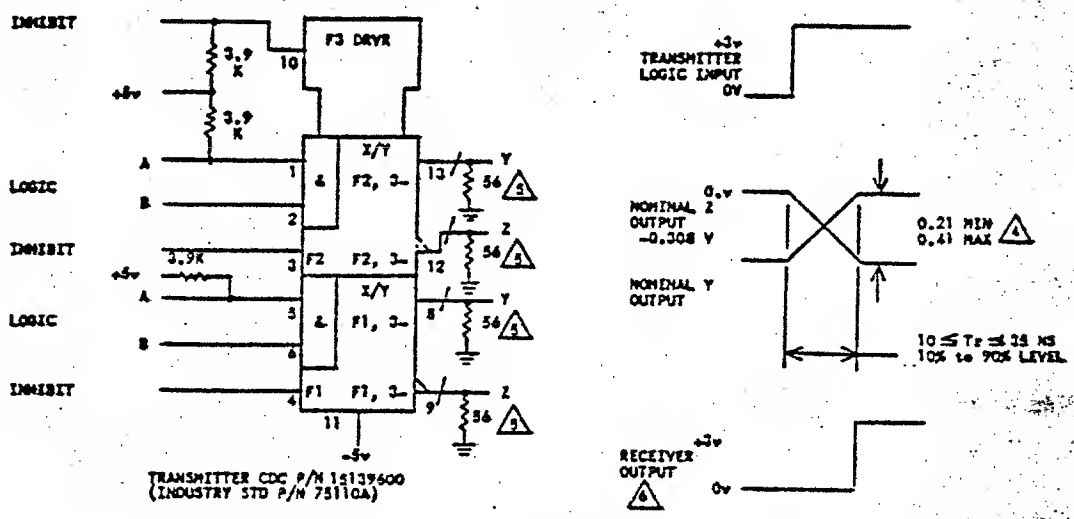
Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised immediately upon sensing index or sector. During a record update, Write Gate is raised within two bits of the last bit of an address, but no closer than 1 bit.



1. CABLE SHALL BE FLAT CABLE WITH CHARACTERISTIC IMPEDANCE 130 ±13 OHMS, CDC P/N 77364300 OR EQUIVALENT.
2. FOR LOGIC LEVELS AND TRUTH TABLE, SEE FIGURES 1, 2 AND 3.
3. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

FIGURE 1. TYPICAL READ/WRITE DATA AND CLOCK TRANSMITTER AND RECEIVER



LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	F2	F1	Y	Z
L or H	L or H	L	L or H	H	3
L or H	L or H	L or H	L	H	3
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

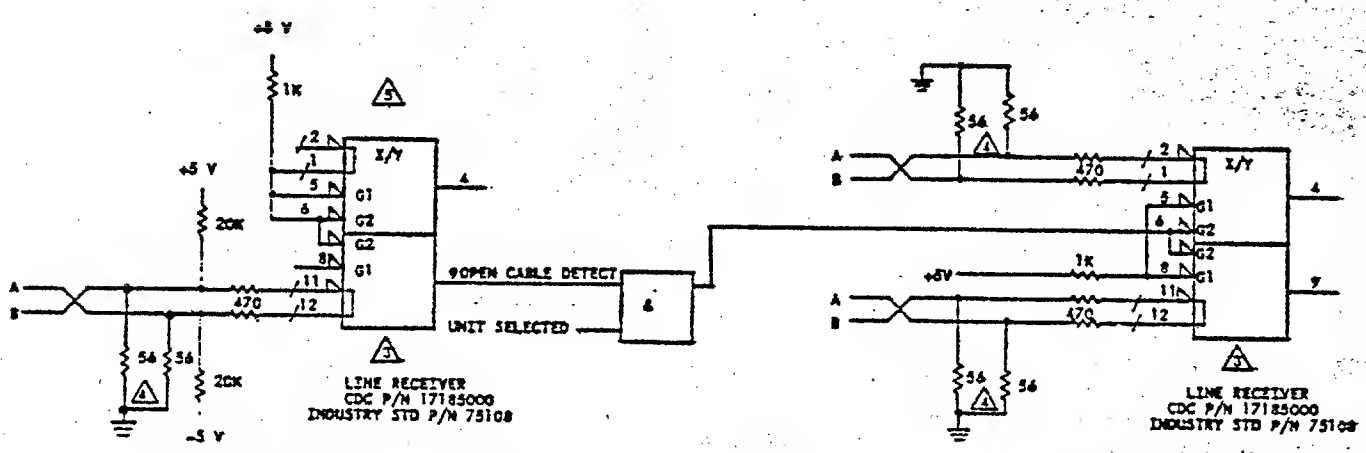
TRUTH TABLE

5105A

NOTES:

1. OUTPUT LEVELS - L = MOST NEGATIVE LEVEL
   H = LEAST NEGATIVE LEVEL
2. INPUT LEVELS - H = MOST POSITIVE LEVEL
   L = LEAST POSITIVE LEVEL
3. THIS IS AN INDETERMINATE INSTRUCTION WHEN SENSED BY AN ACTIVE (SELECTED) RECEIVER.
4. VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF 11 ±3 MA, AND TERMINATING RESISTOR RANGE OF 56 ±5% OHMS.
5. TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY. REFER TO SINGLE AND DUAL CHANNEL INTERFACE ILLUSTRATION, AND THE TERMINATOR PARAGRAPH.
6. RECEIVER INPUTS A AND B ARE CONNECTED TO TRANSMITTER OUTPUTS Y AND Z RESPECTIVELY.

FIGURE 2. CONTROL LINE TRANSMITTER



ST068

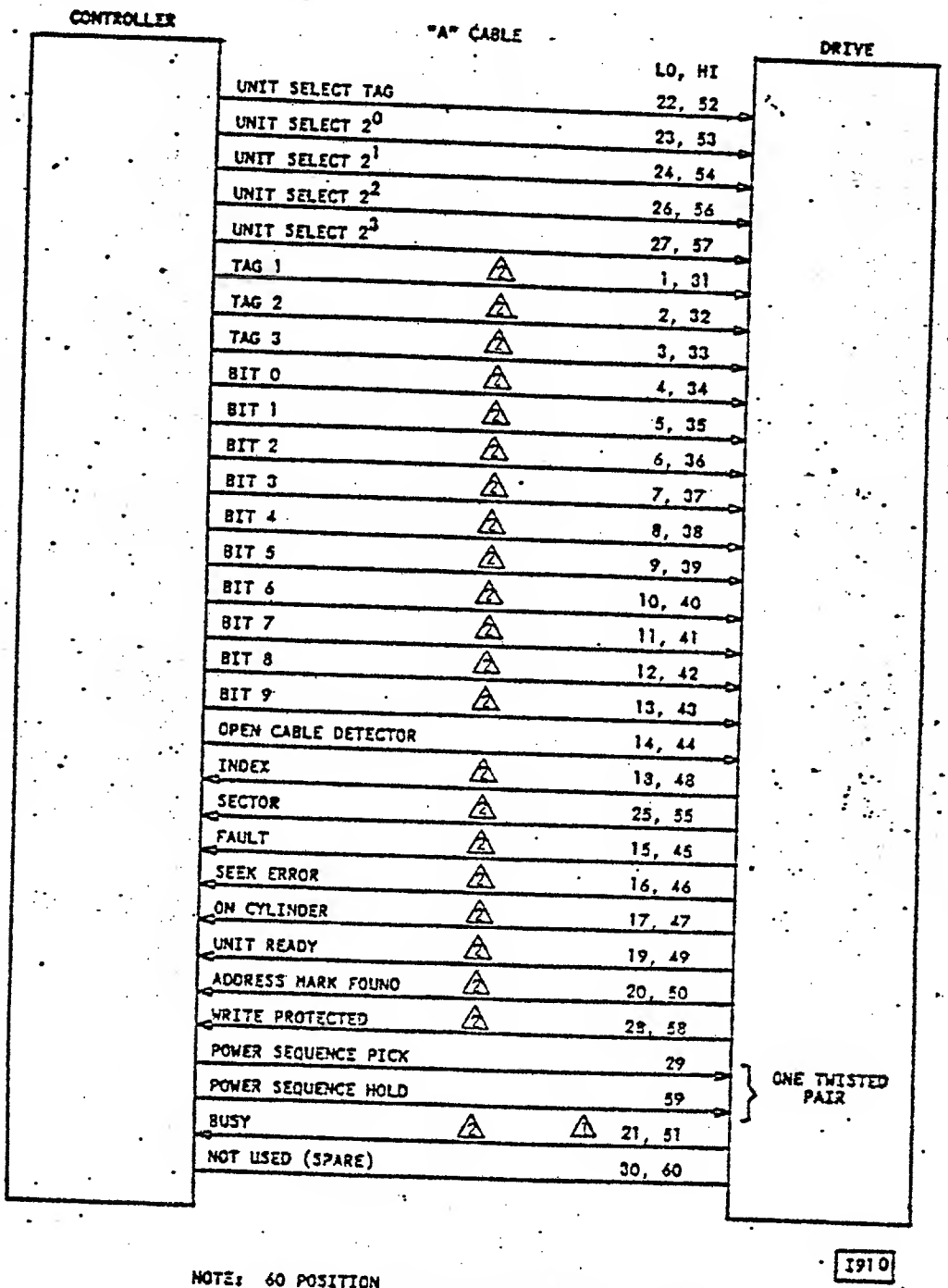
DIFFERENTIAL INPUTS	INHIBIT		OUTPUT
	G1	G2	
$V_A - V_B \geq 25mv$	L or H	L or H	H
$\lvert V_A - V_B \rvert < 25mv$	L or H	L	H
	L	L or H	H
	H	H	IND.
$V_B - V_A \geq 25mv$	L or H	L	H
	L	L or H	H
	H	H	L

LINE RECEIVER TRUTH TABLE

NOTES:

1. 20K OHM RESISTORS ARE TYPICAL VALUES.
2. ALL VALUES IN OHMS UNLESS INDICATED OTHERWISE.
3. A BIAS NETWORK SHOULD BE USED TO PREVENT FALSE STATUS OR INTERRUPT CONDITIONS WHEN DRIVE POWER IS OFF AT CONTROLLER END OF UNIT SELECTED AND SEEK END SIGNALS.
4. TERMINATING RESISTORS ARE LOCATED:
   A. ON LOGIC CARD FOR "B" CABLE LINES.
   B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
5. SEE 1.2.2.7 FOR DESCRIPTION OF OPEN CABLE DETECT SIGNAL.

FIGURE 3. CONTROL LINE RECEIVER



NOTE: 60 POSITION
28 AWG, 30 PAIR, TWISTED-STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT

1 DUAL CHANNEL UNITS ONLY.

2 GATED BY UNIT SELECTED.

FIGURE 4. TAB BUS I/O INTERFACE

BUS	TAG 1 IN CYLINDER ADDRESS	TAG 2 IN HEAD SELECT	TAG 3 IN CONTROL SELECT	UNIT SELECT
Bit 0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	Servo Offset Plus	
3	2^3	2^3	Servo Offset Minus	
4	2^4	2^4	Fault Clear	
5	2^5		AM Enable	
6	2^6		RTZ	
7	2^7		Data Strobe Early	
8	2^8		Data Strobe Late	
9	2^9		Release (1)	(1) Priority Select

(1) DUAL CHANNEL ONLY

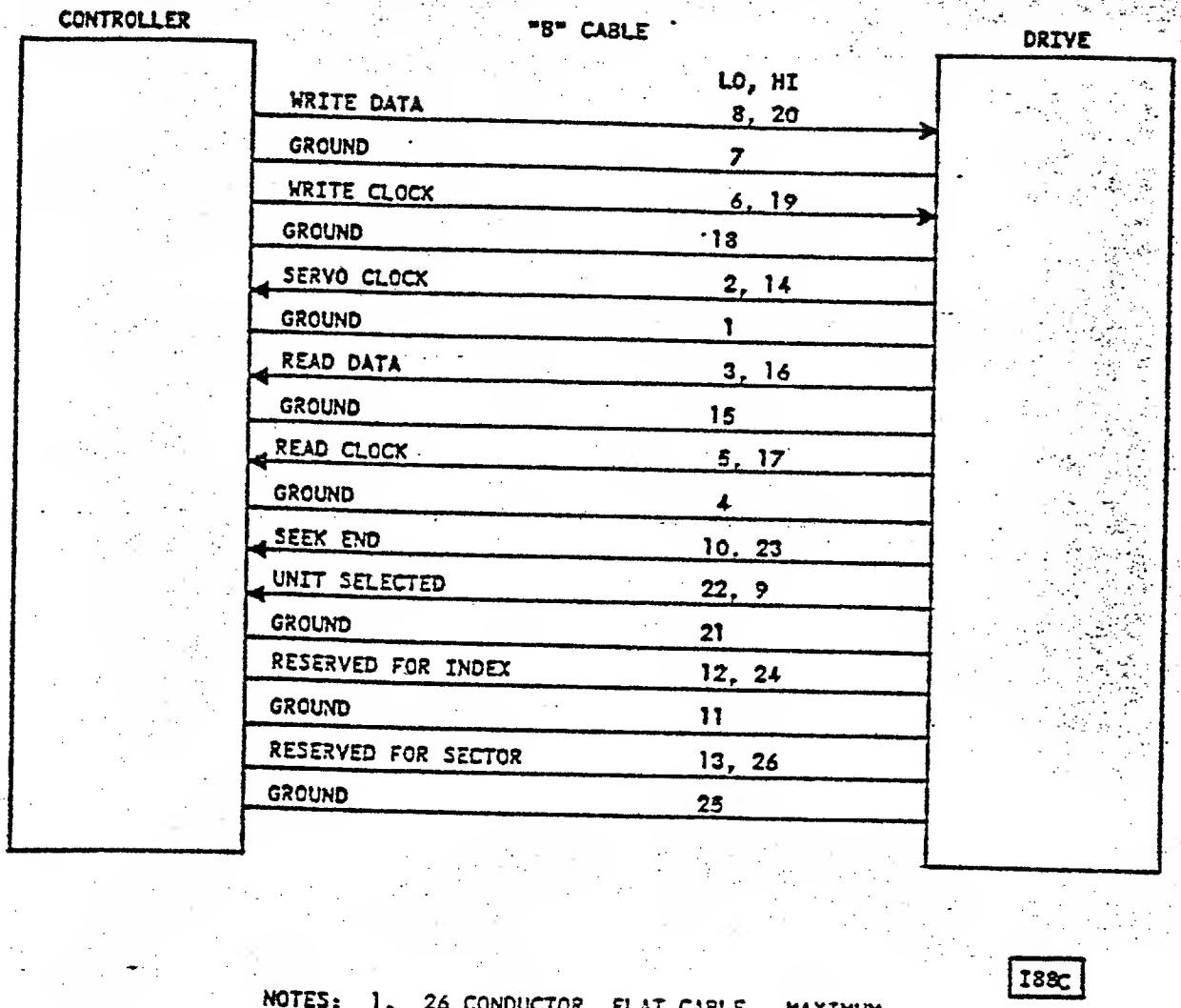
NOTE: FOR CMD SEE FIGURE 5B.

FIGURE 5A. TAG BUS DECODE SMD/MMD

BUS	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD/VOLUME SELECT	TAG 3 CONTROL SELECT
BIT 0	2^0	2^0	WRITE GATE
1	2^1	2^1	READ GATE
2	2^2	2^2	SERVO OFFSET PLUS
3	2^3		SERVO OFFSET MINUS
4	2^4		FAULT CLEAR
5	2^5		AM ENABLE
6	2^6		RTZ
7	2^7		DATA STROBE EARLY
8	2^8		DATA STROBE LATE
9	2^9	2^9 (1)	

(1) THIS BIT IS VOLUME ADDRESS WHICH IS STORED IN A BISTABLE WITHIN THE 9448 DRIVE. THE STORED VOLUME ADDRESS AND "TAG 1" RESULT IN A VOLUME SELECT IF THE CYLINDER ADDRESS IS VALID. (REFER TO FLOW CHART FOR TIMING.) A ZERO DENOTES THE REMOVEABLE CARTRIDGE AND A ONE DENOTES THE FIXED DISKS.

FIGURE 5B. TAG BUS DECODE - CMD



NOTES: 1. 26 CONDUCTOR FLAT CABLE. MAXIMUM LENGTH - 50 FT.

2. NO SIGNALS GATED BY UNIT SELECTED.

FIGURE 6. "B" CABLE INTERFACE

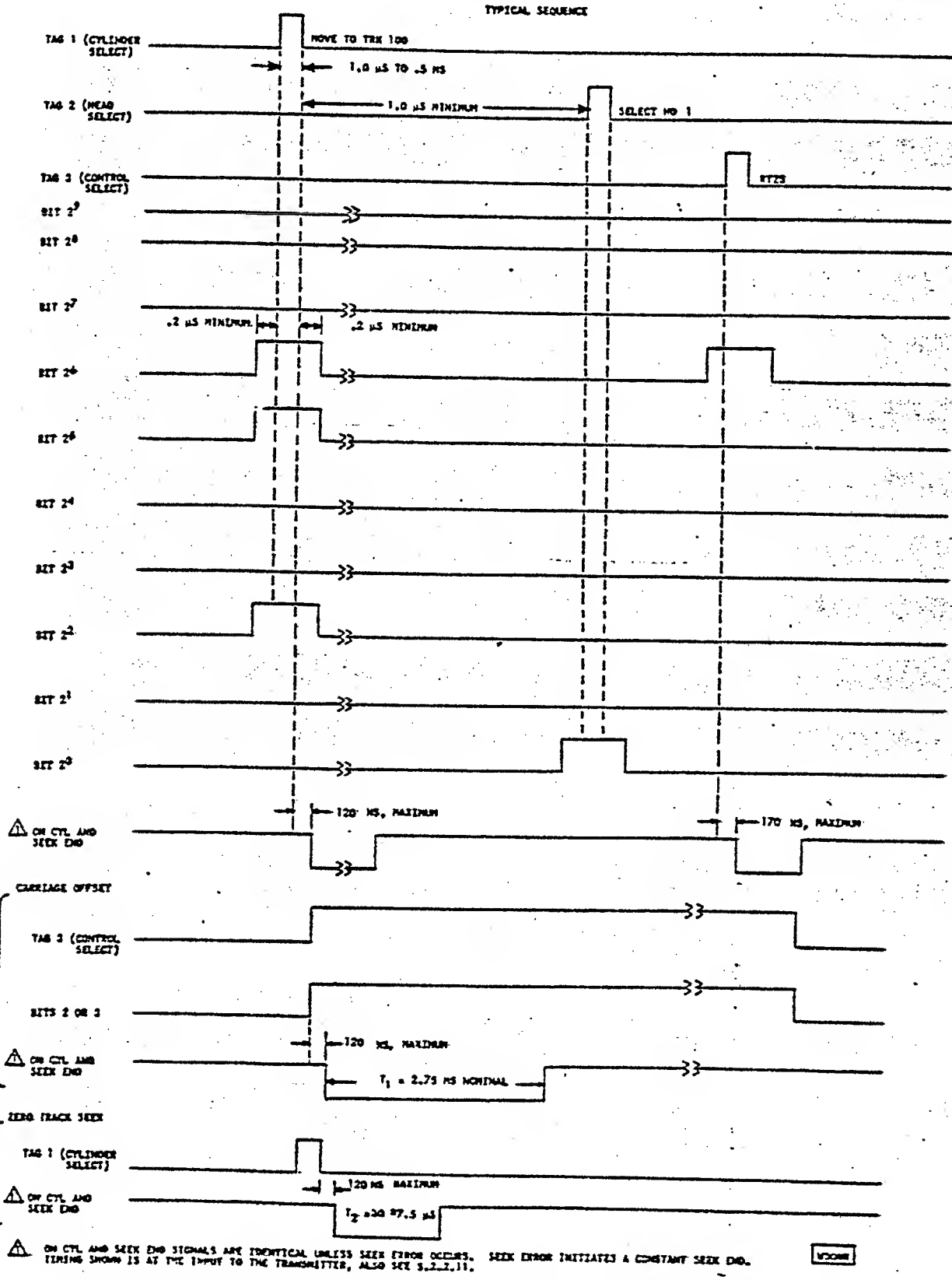
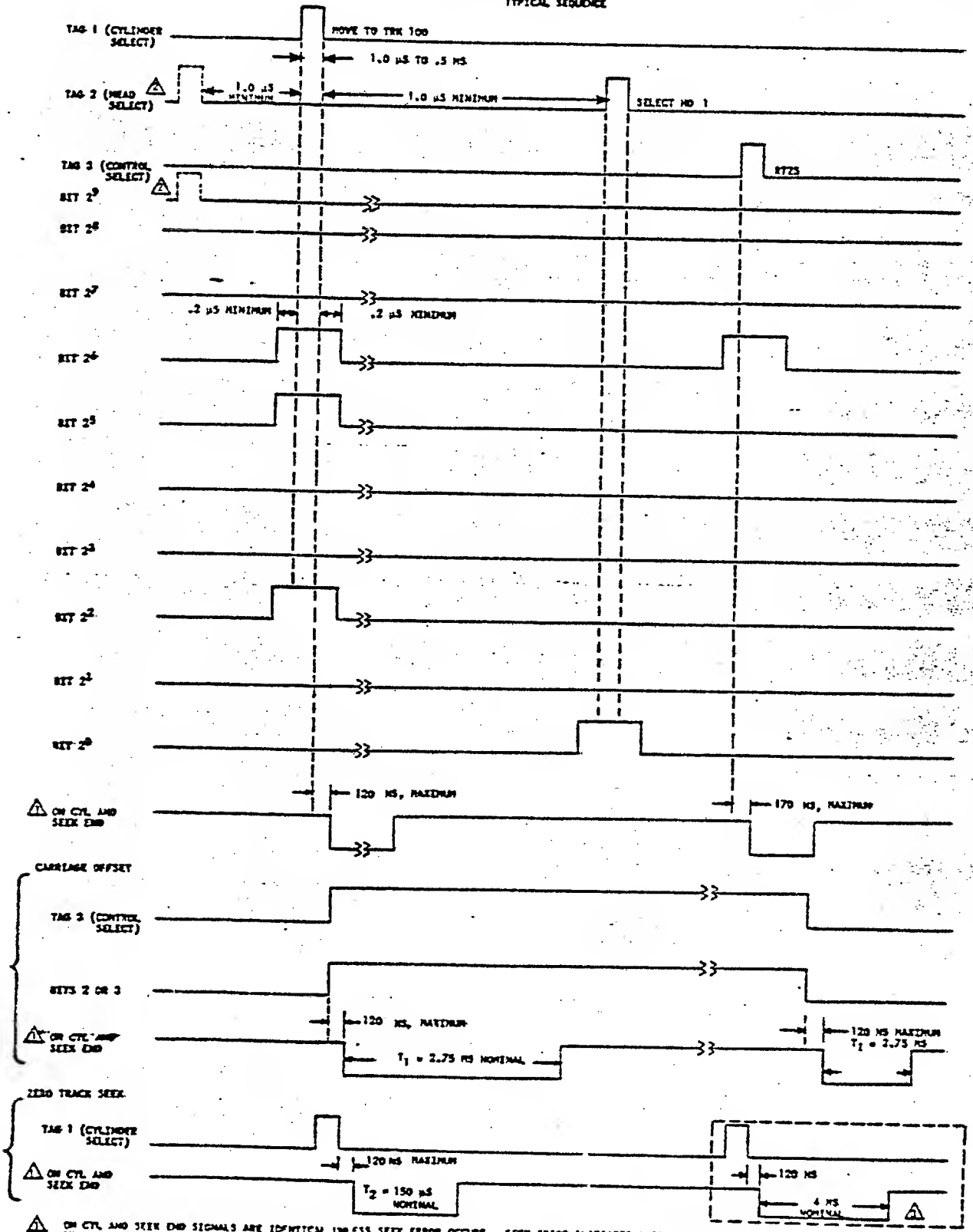


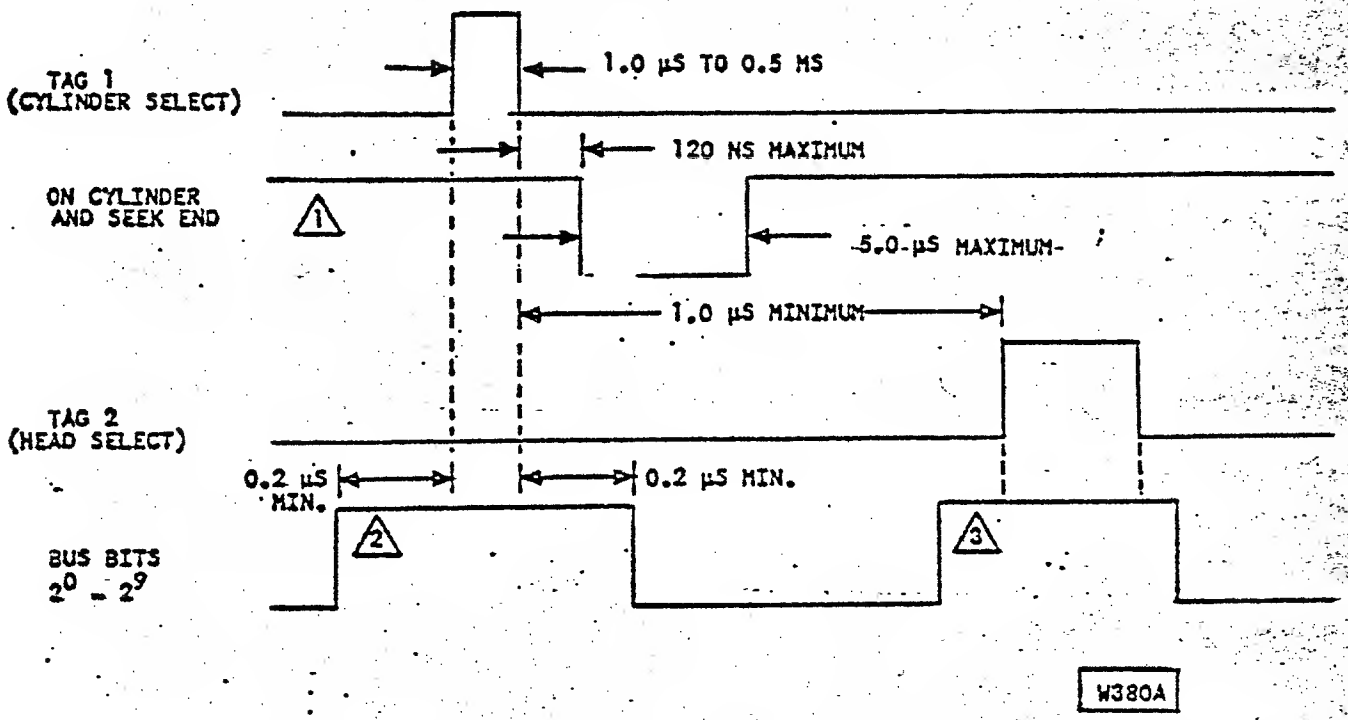
FIGURE 7A. TAG AND BUS TIMING - SMD AND MMD (MOVING HEADS)

NORMANDALE OPERATIONS



1. ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER, ALSO SEE 8.2.2.11.
2. TAG AND BUS TIMING REQUIREMENTS FOR A VOLUME CHANGE.
3. ZERO TRACK SEEK TIMING WITH VOLUME CHANGE.

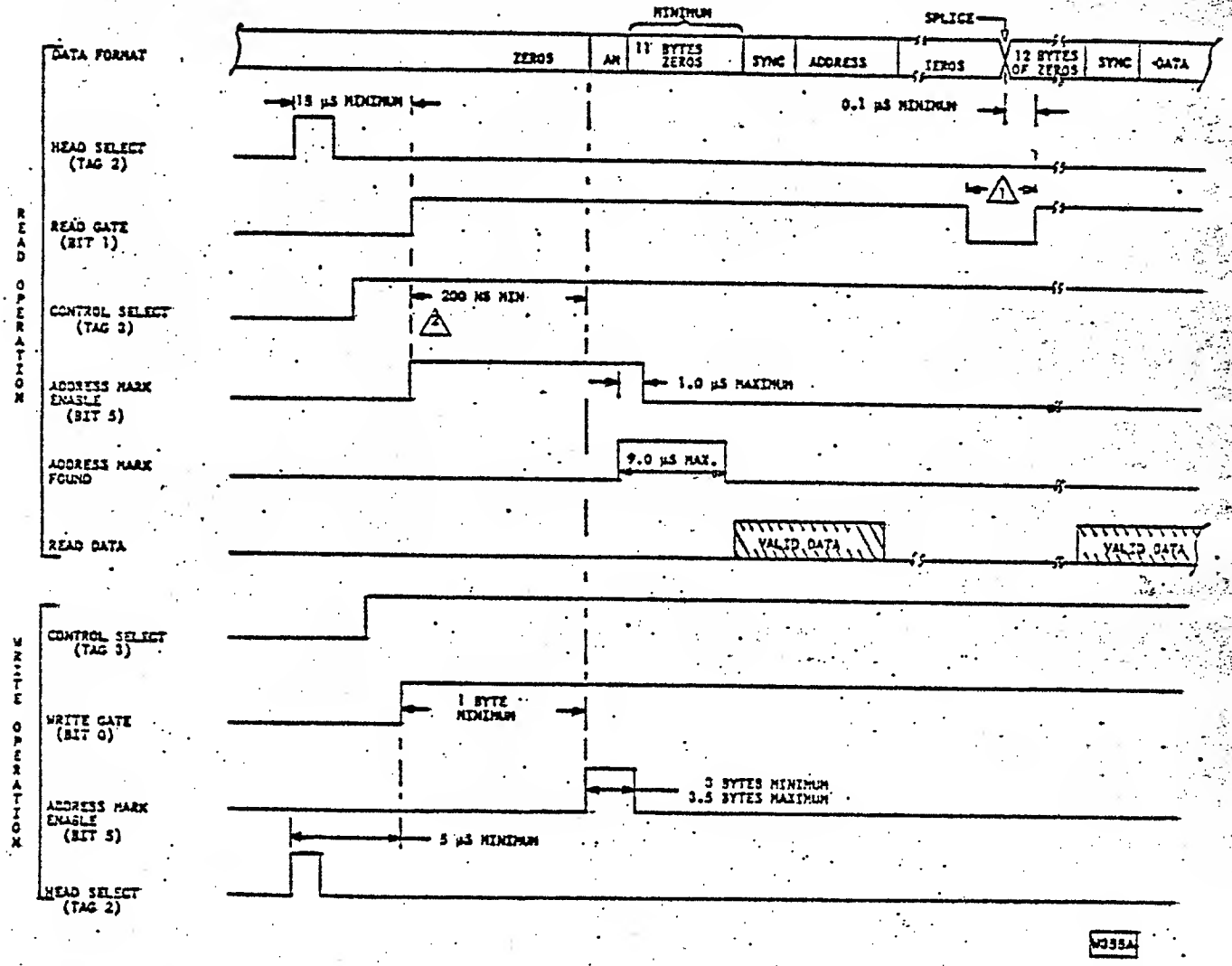
FIGURE 78. TAG AND BUS TIMING - CMD



NOTES:

1. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER.
2. CYLINDER ADDRESSES 896-907 FOR FIXED HEAD (12 AND 24 MB).
   CYLINDER ADDRESSES 896/905/915 FOR FIXED HEAD (80 MB).
3. HEAD ADDRESSES 0 - 4 FOR FIXED HEAD.
4. TAG 1 and TAG 2 MAY BE ISSUED IN EITHER ORDER PROVIDING 1.0 µS MINIMUM TIMING IS ALLOWED BETWEEN COMMANDS.
5. HEAD SELECT MUST BE REISSUED WHEN SWITCHING BETWEEN FIXED AND MOVEABLE STORAGE.

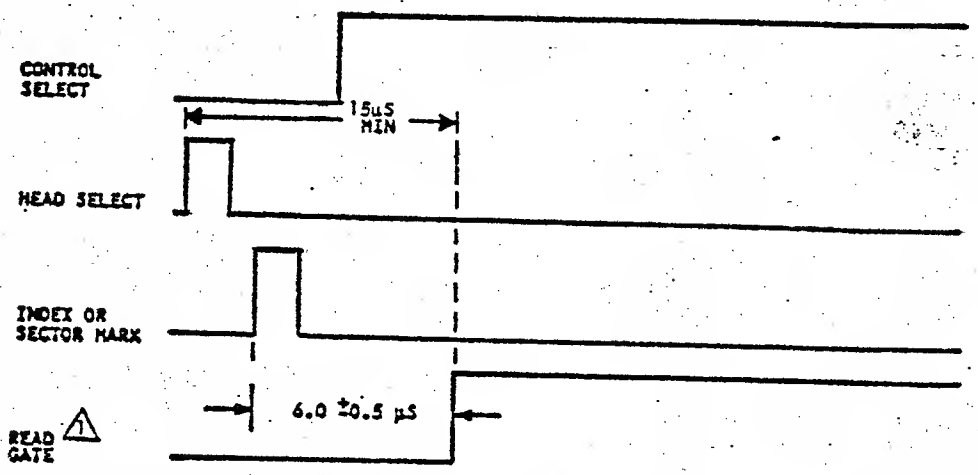
FIGURE 7C. FIXED HEAD TAG/BUS TIMING - MMD



NOTES: ⚠1 READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE (EXAMPLE) CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

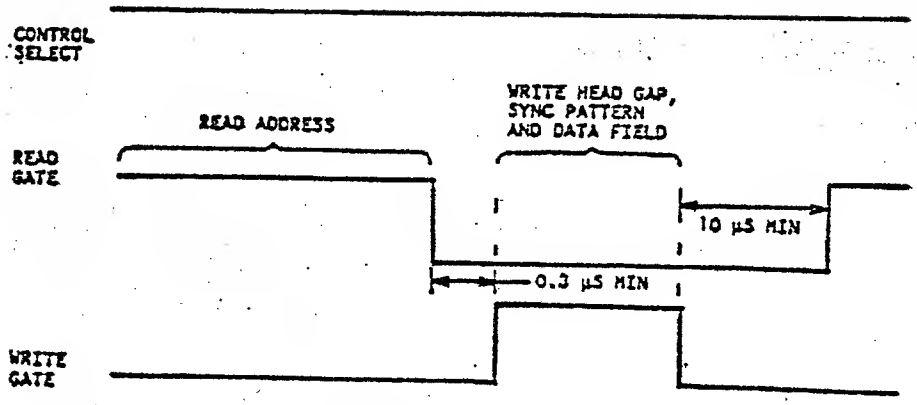
⚠2 ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUSLY WITH READ GATE.

FIGURE 8A. TYPICAL READ/WRITE TIMING WITH ADDRESS MARK



1 IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR, READ GATE MUST NOT OCCUR LATER THAN 6.0 ±0.5µS AFTER THE LEADING EDGE OF INDEX OR SECTOR.

A. TYPICAL READ CONTROL TIMING



B. TYPICAL WRITE CONTROL TIMING

W359A

FIGURE 88. CONTROL TIMING

FIGURE 9. SAMPLE PRIORITY SELECT TIMING

This Document contains preliminary Information and is subject to change.

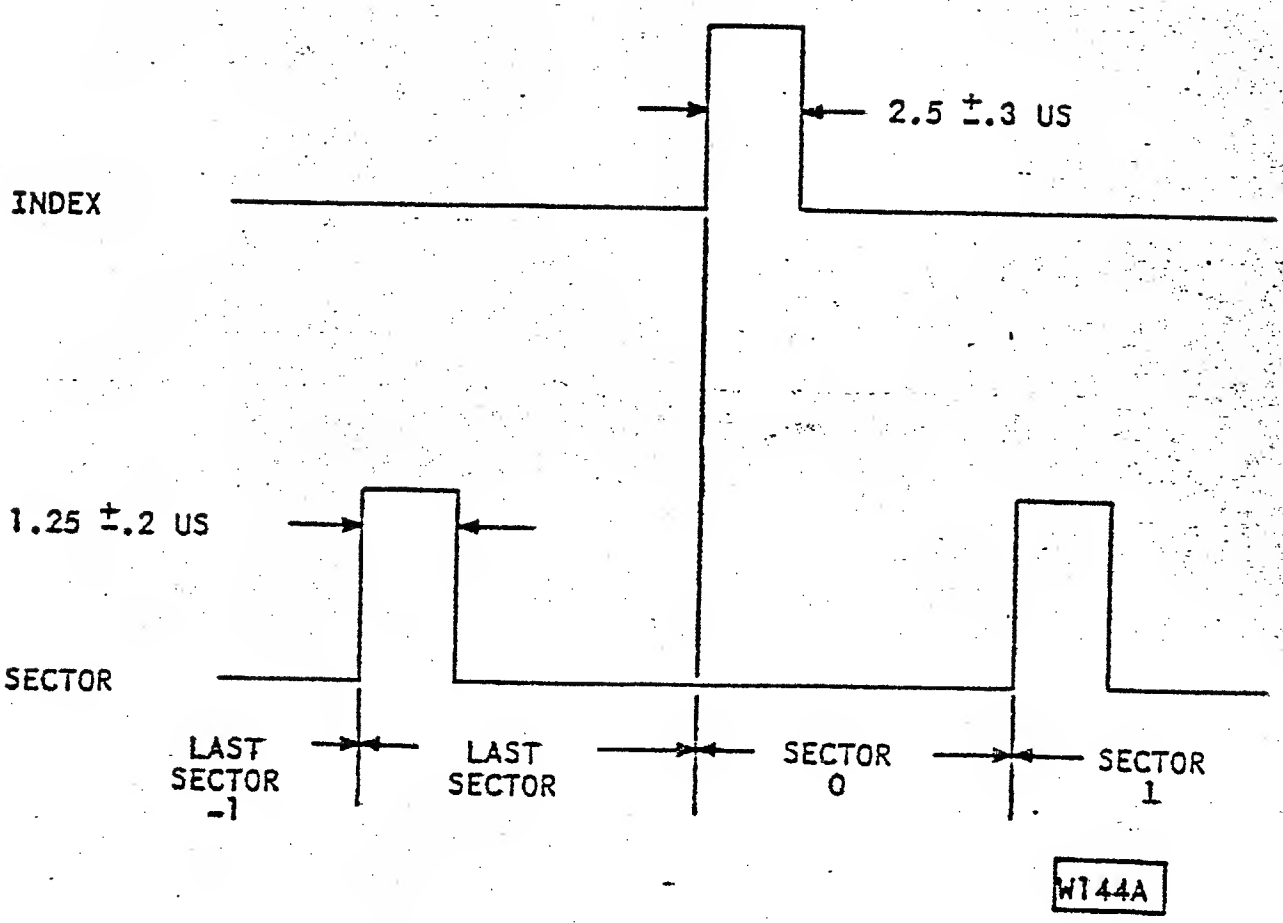


FIGURE 10. INDEX AND SECTOR TIMING

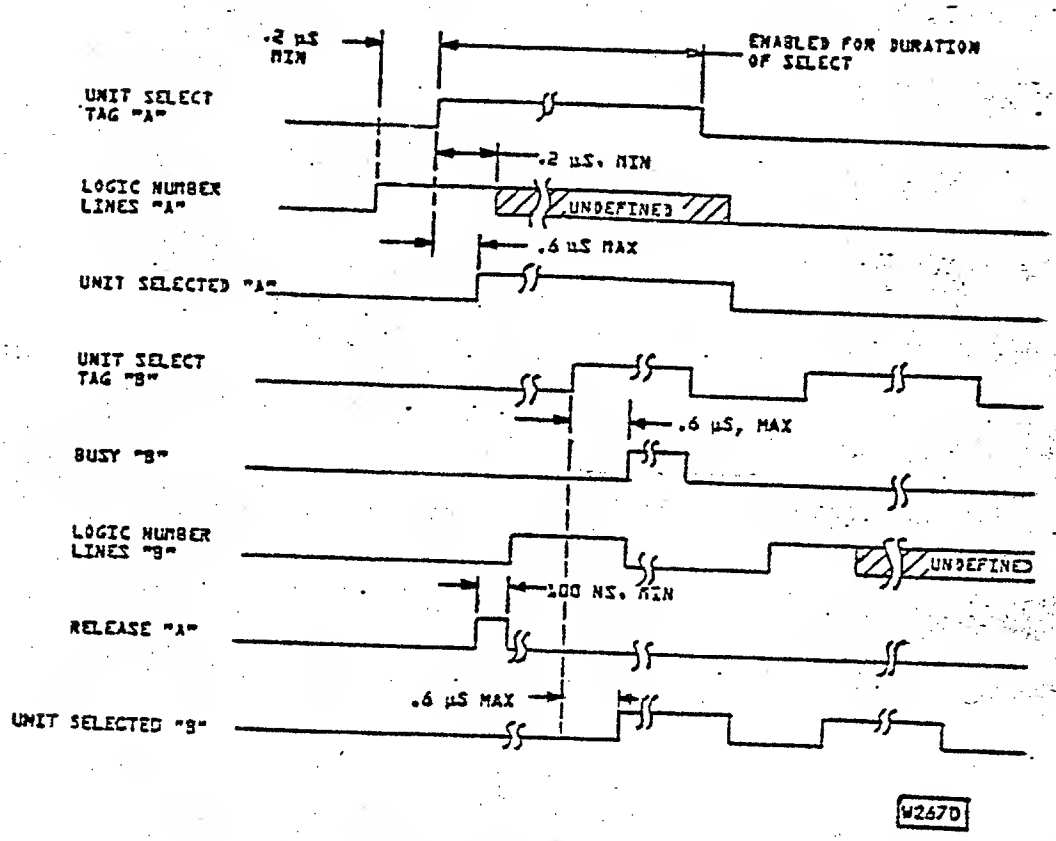


FIGURE 11. LOGIC NUMBER SELECT AND TIMING DIAGRAM

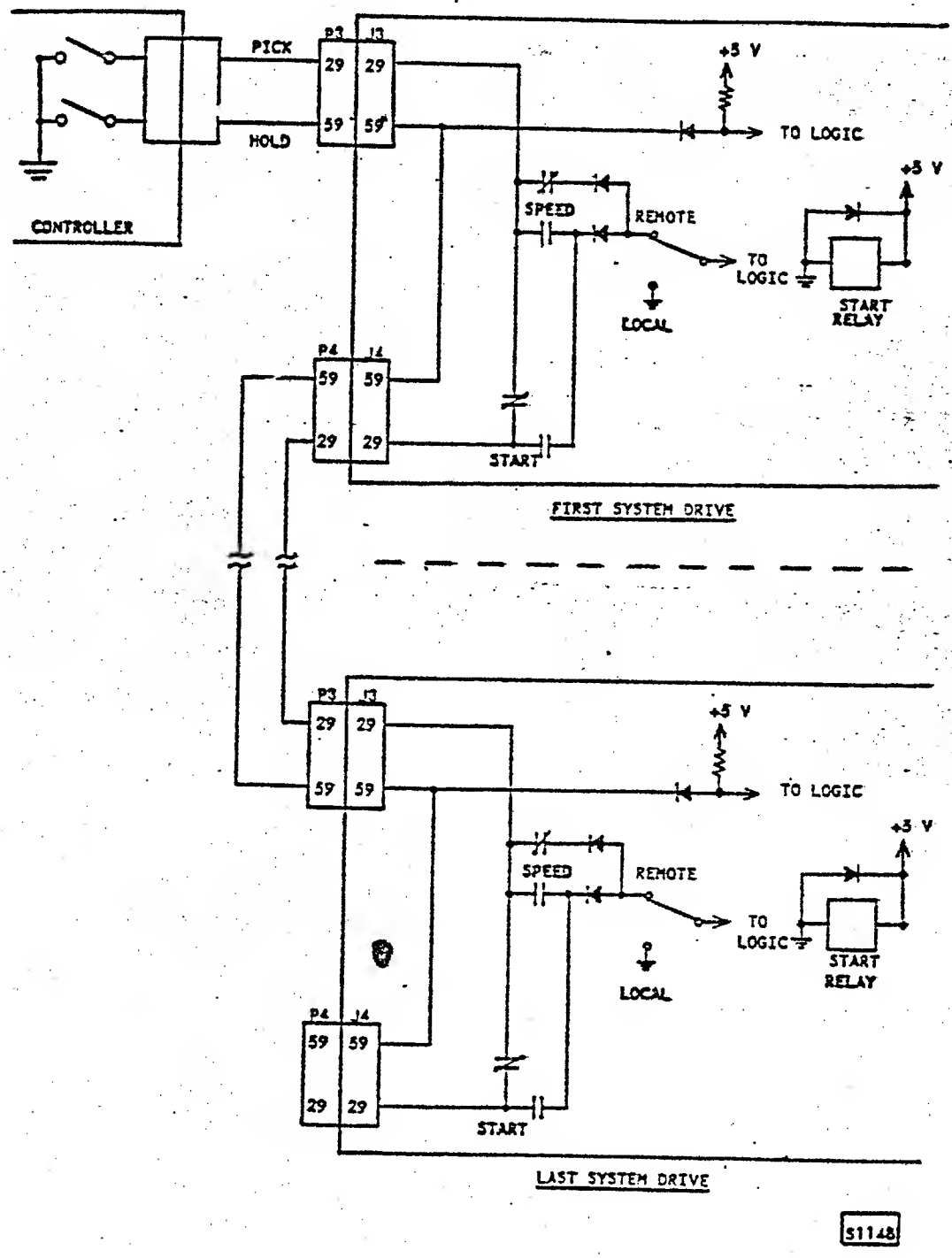


FIGURE 12A. SEQUENCE POWER LINES - MMD

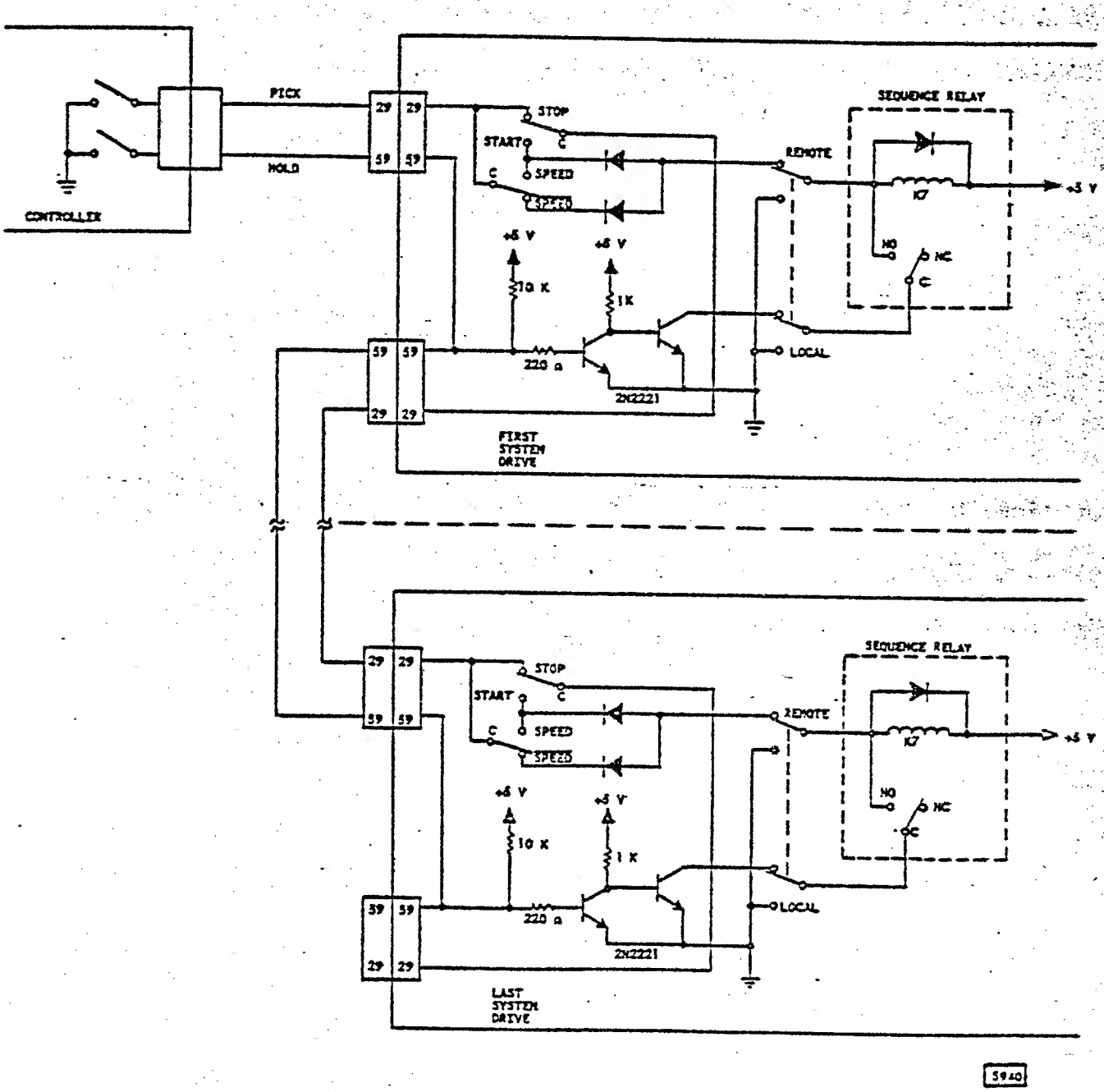


FIGURE 128. 9760/9762 SEQUENCE POWER LINES

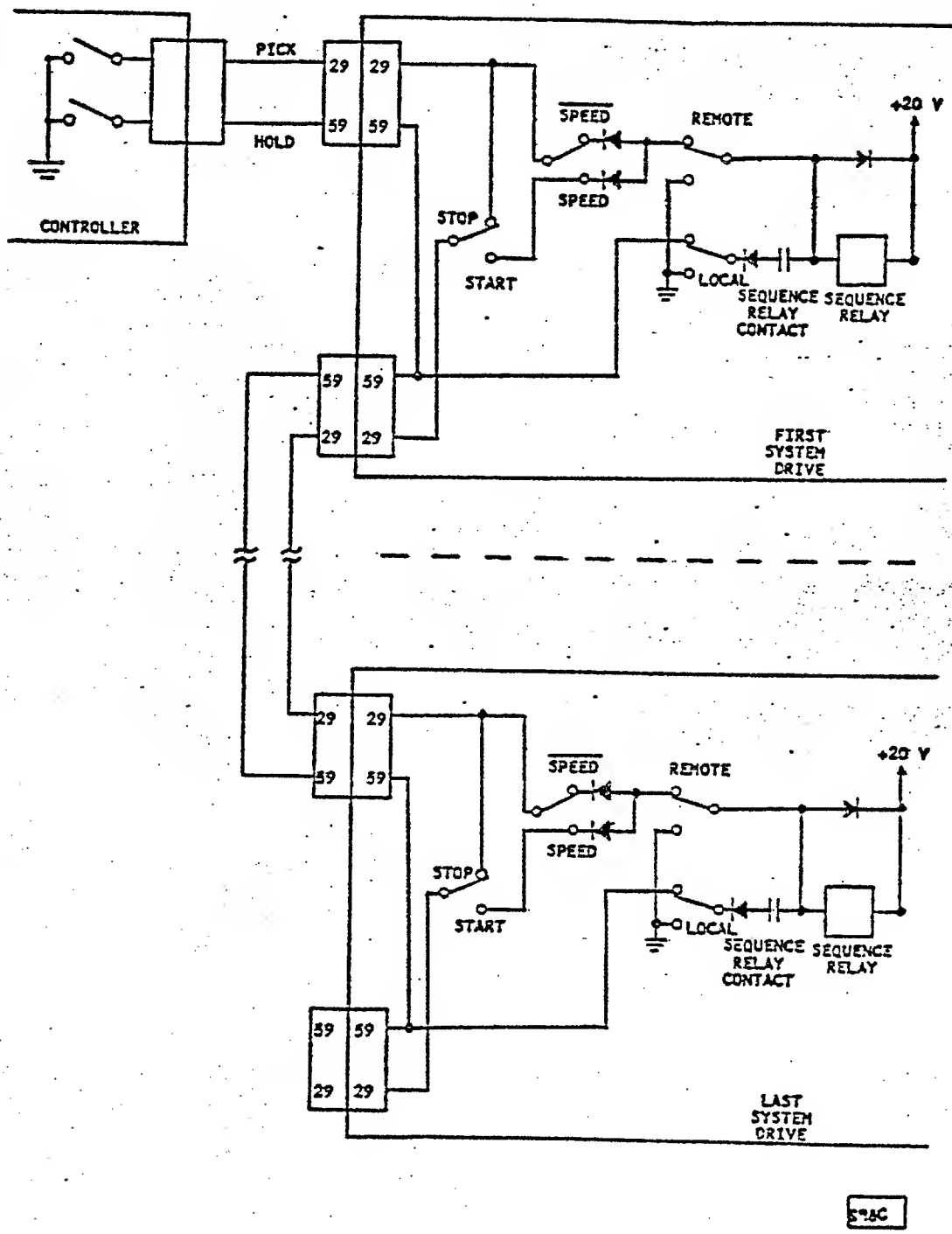


FIGURE 12C. 9764/9766 SEQUENCE POWER LINES

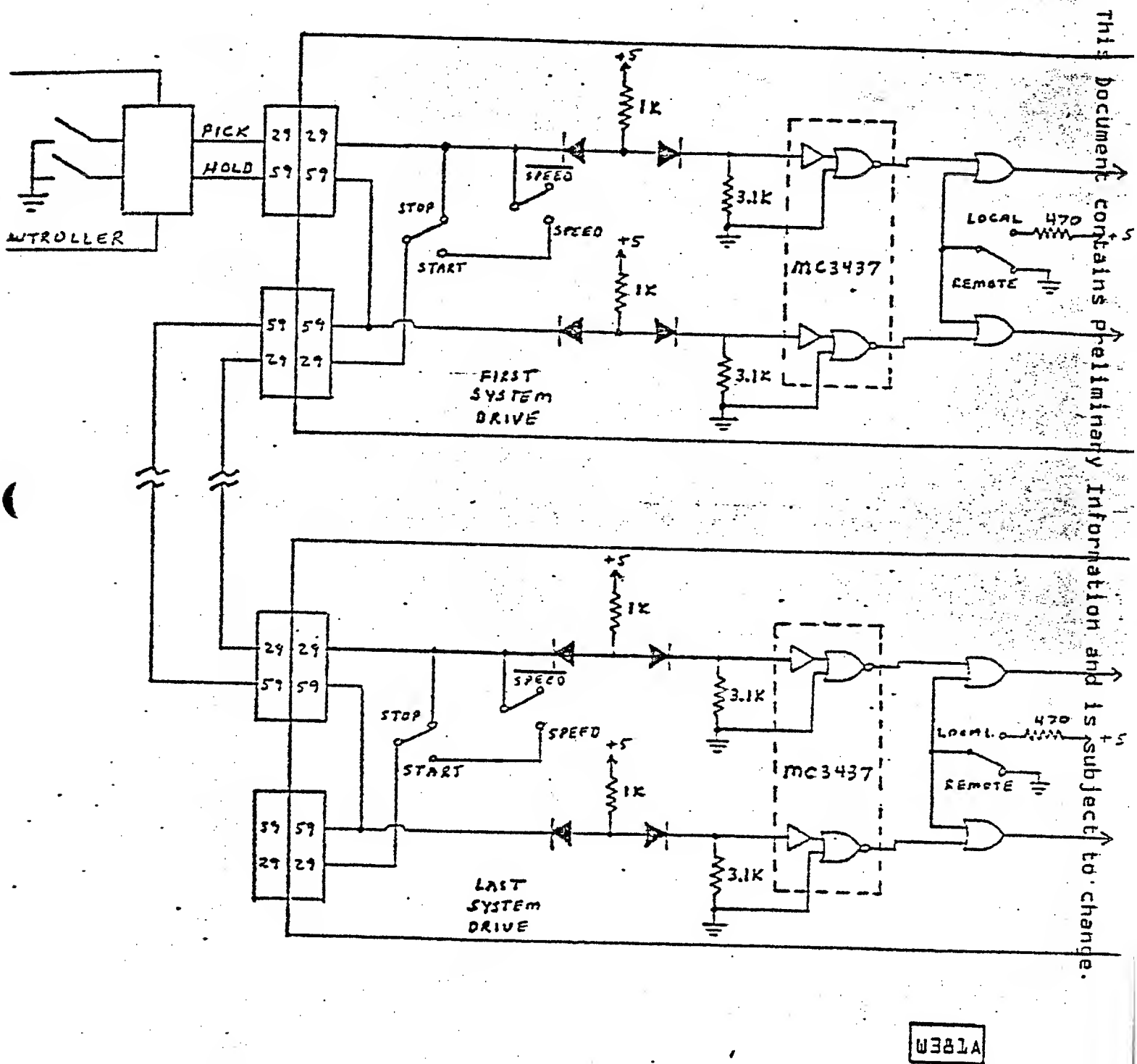
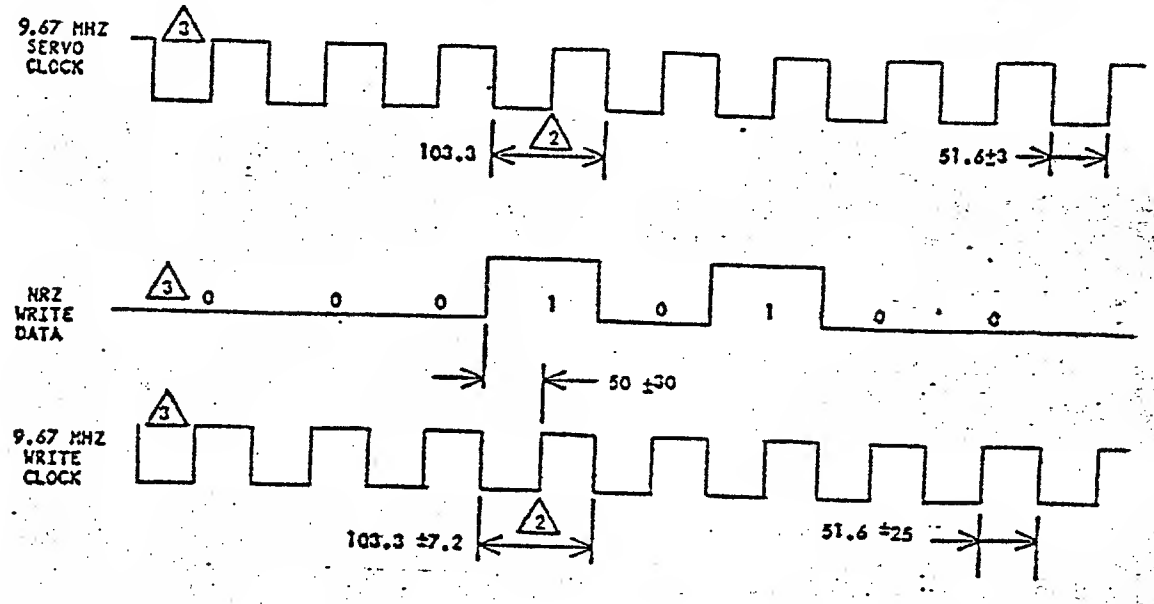
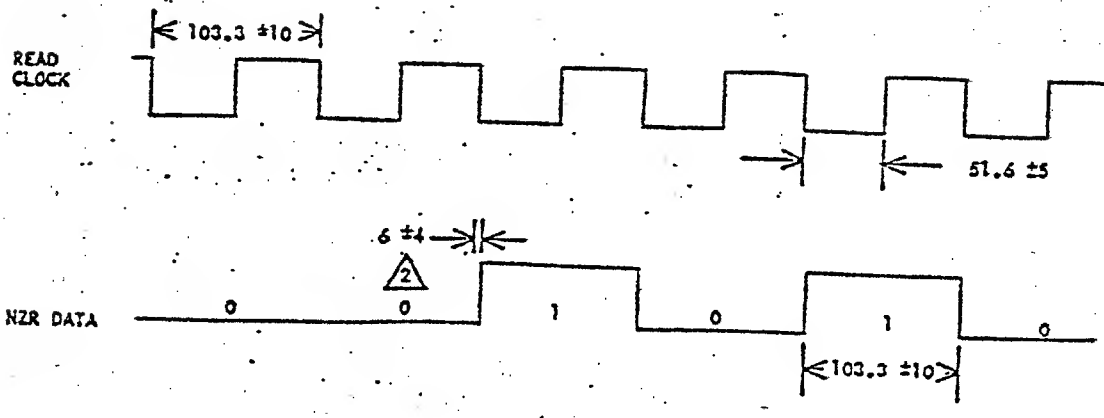


FIGURE 12D. SEQUENCE POWER LINES - CMD



NOTES:

1. ALL TIMES IN NS.
2. SIMILAR PERIOD SYMMETRY SHALL BE ±2 NS. AT I/O CONNECTOR IN DRIVE, SPEED VARIATION TOLERANCE SHALL BE -5%, +4% OF PERIOD WHICH INCLUDES SPINDLE SPEED TOLERANCE AND DIBIT DROPOUT WHILE CARRIAGE IS MOVING.
3. AT I/O CONNECTOR IN CONTROLLER.

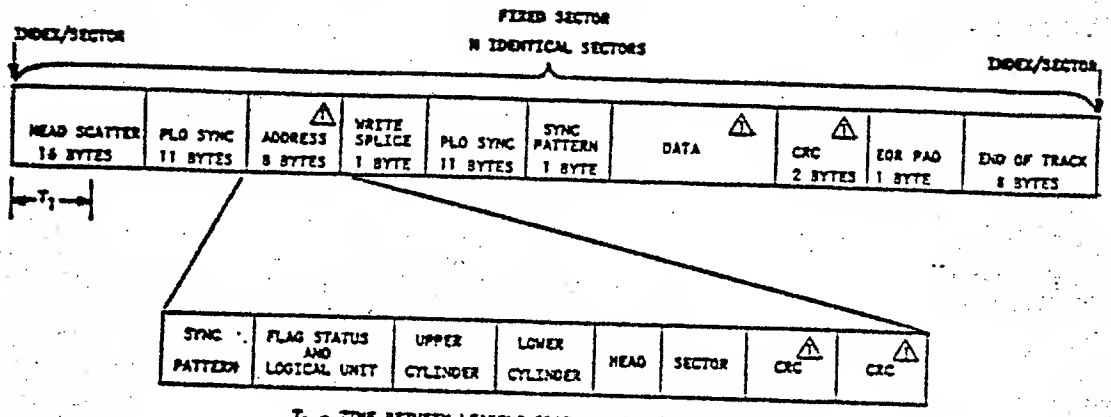


NOTES:

1. ALL TIMES IN NS..
2. NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

W384A

FIGURE 13B. NZR DATA AND READ CLOCK TIMING



T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

01358-1

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

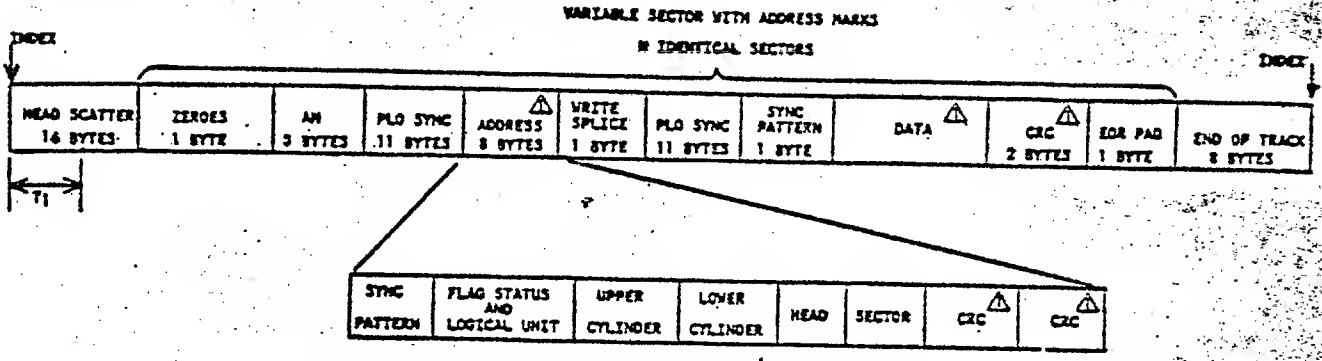
$$\text{DATA FIELD} = \frac{20\,160}{64} - 59 = 256\ \frac{\text{BYTES}}{\text{SECTOR}}$$

DATA = 256 BYTES/SECTOR

$$\%\ \text{EFFICIENCY} = \frac{256 \times 64}{20\,160} \times 100 = 81\%$$

⚠ THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 14A. FIXED SECTOR FORMAT



T_1 = TIME BETWEEN LEADING EDGE OF INDEX AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

D134C

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK} - \text{MECHANICAL TOLERANCES}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160 \frac{\text{BYTES}}{\text{TRACK}} - 24 \frac{\text{BYTES}}{\text{TRACK}}}{64 \frac{\text{SECTORS}}{\text{TRACK}}} - 39 \frac{\text{BYTES}}{\text{SECTOR}} = 275 \frac{\text{BYTES}}{\text{SECTOR}}$$

$$\% \text{ EFFICIENCY} = \frac{275 \times 64}{20\,160} \times 100 = 87\%$$

EXAMPLE NO. 2: WHAT IS NUMBER OF SECTORS USING 256 DATA BYTES?

$$\text{N SECTORS} \quad \frac{20\,160 - 24}{256 + 39} = 68 \text{ SECTORS}$$

$$\% \text{ EFFICIENCY} = \frac{256 \times 68}{20\,160} \times 100 = 86\%$$

⚠ THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 148. VARIABLE SECTOR FORMAT

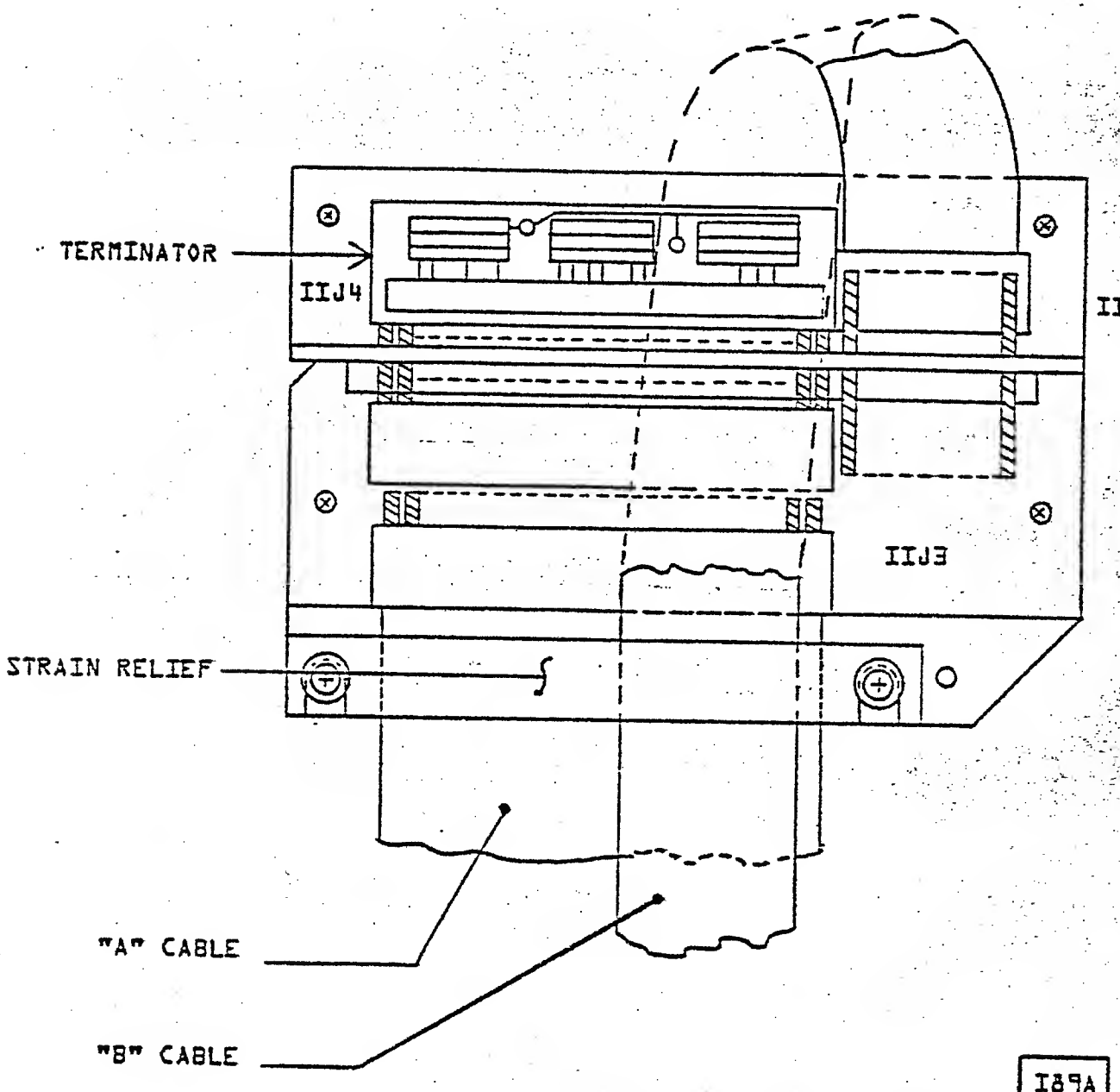
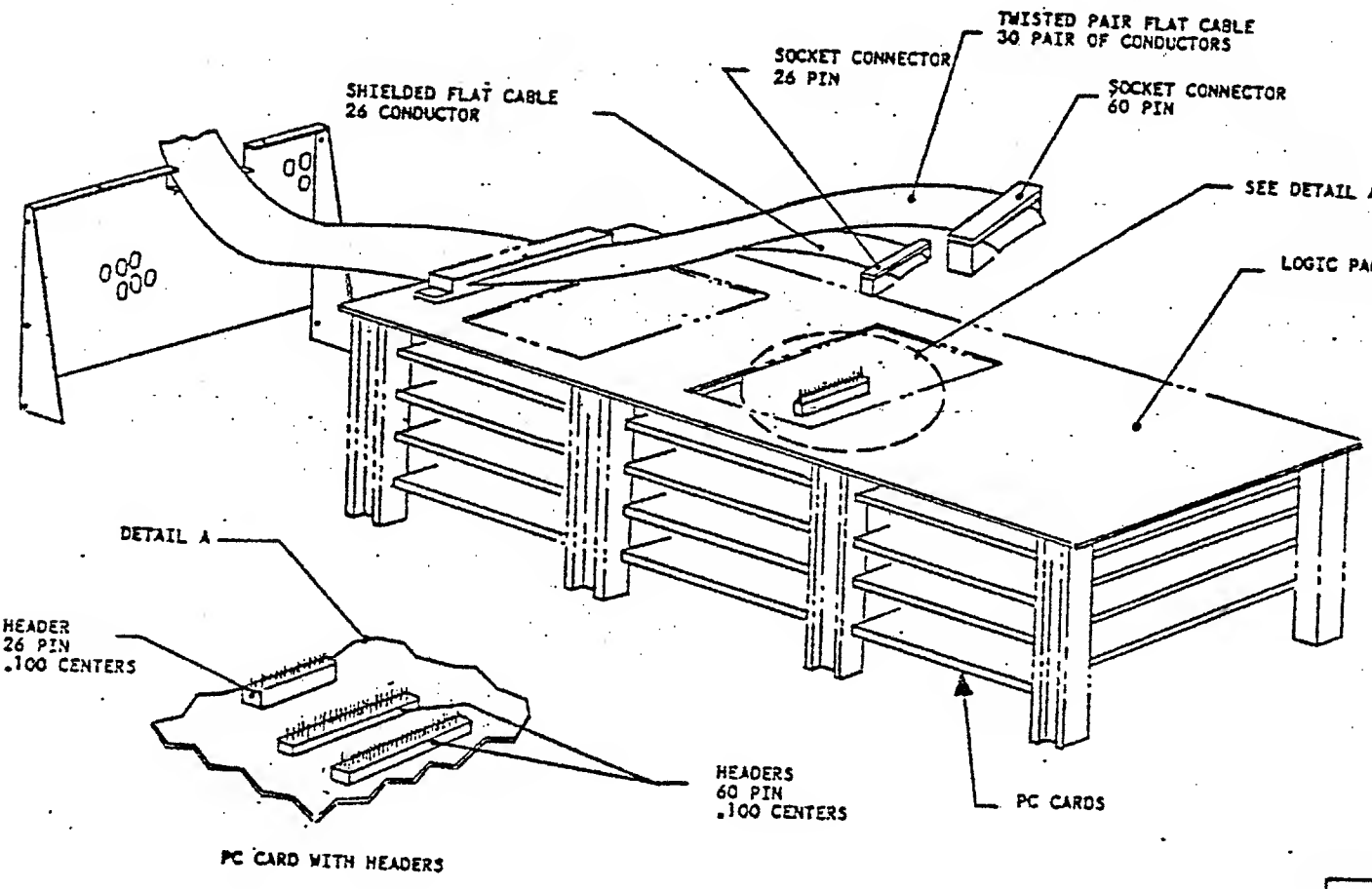
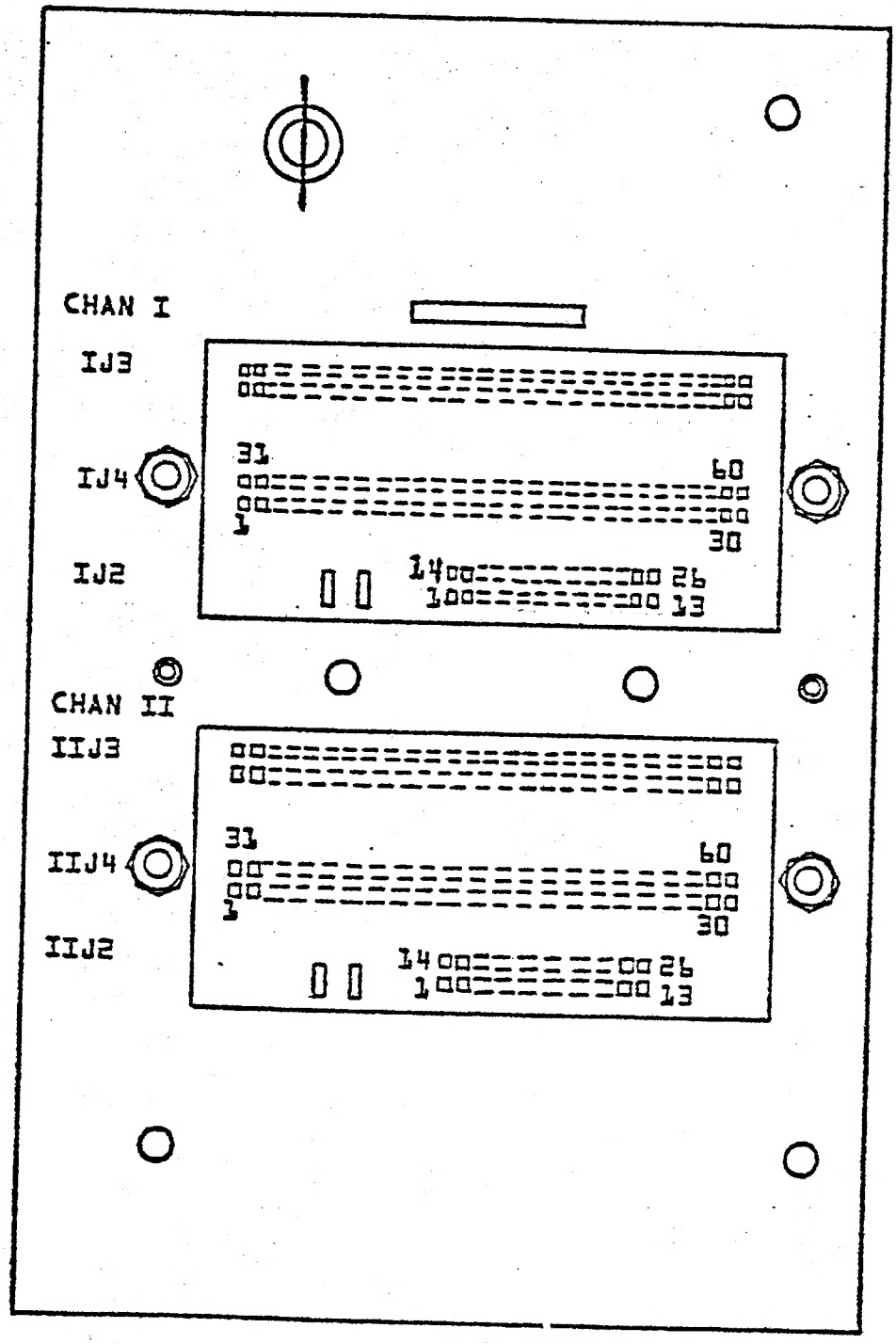


FIGURE 15A. I/O CONNECTORS 9760/9762 SMD



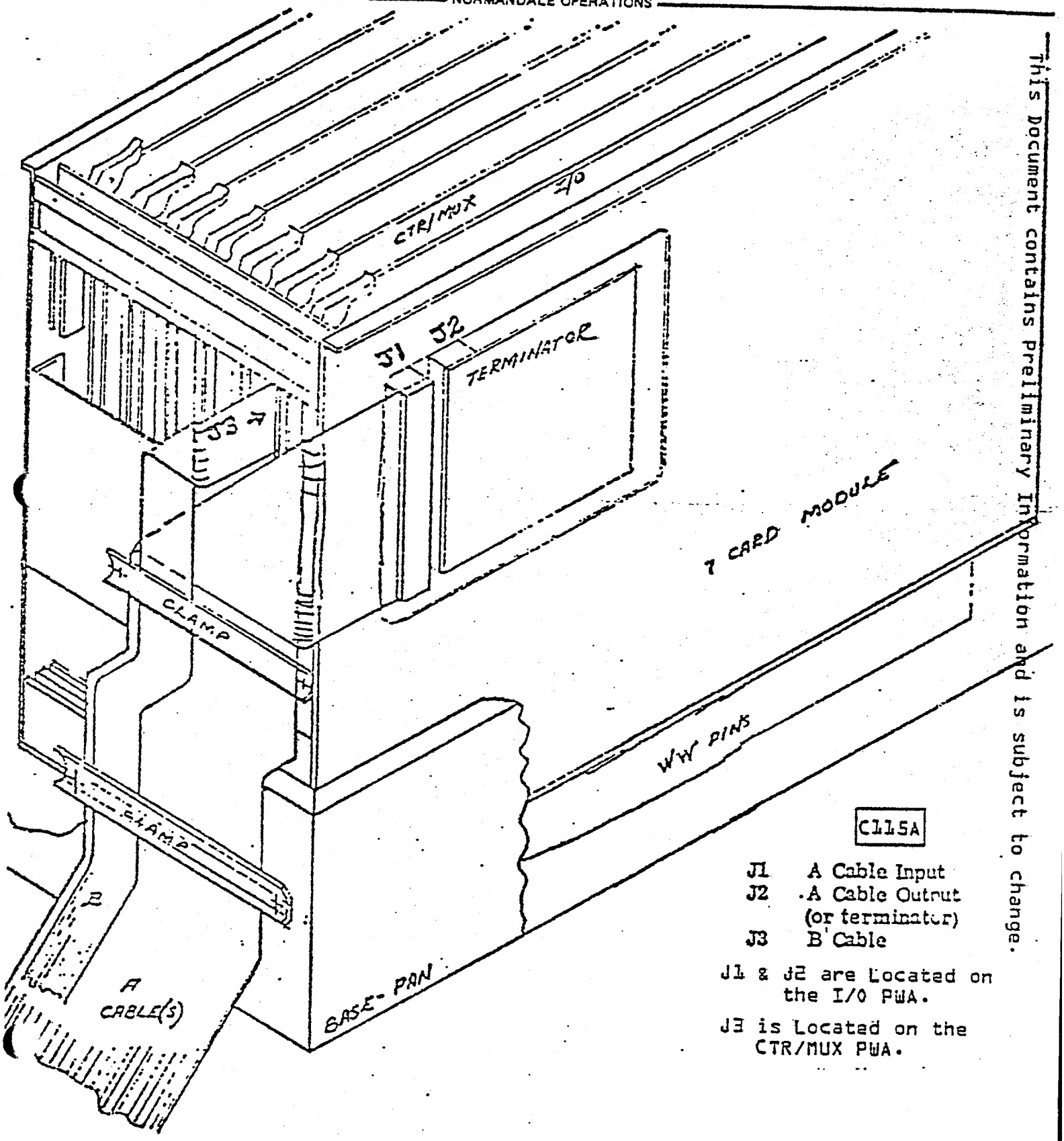
I82E

FIGURE 15B. I/O CONNECTORS MMD



I90A

FIGURE 15C. I/O CONNECTORS 9764/9766 SMD



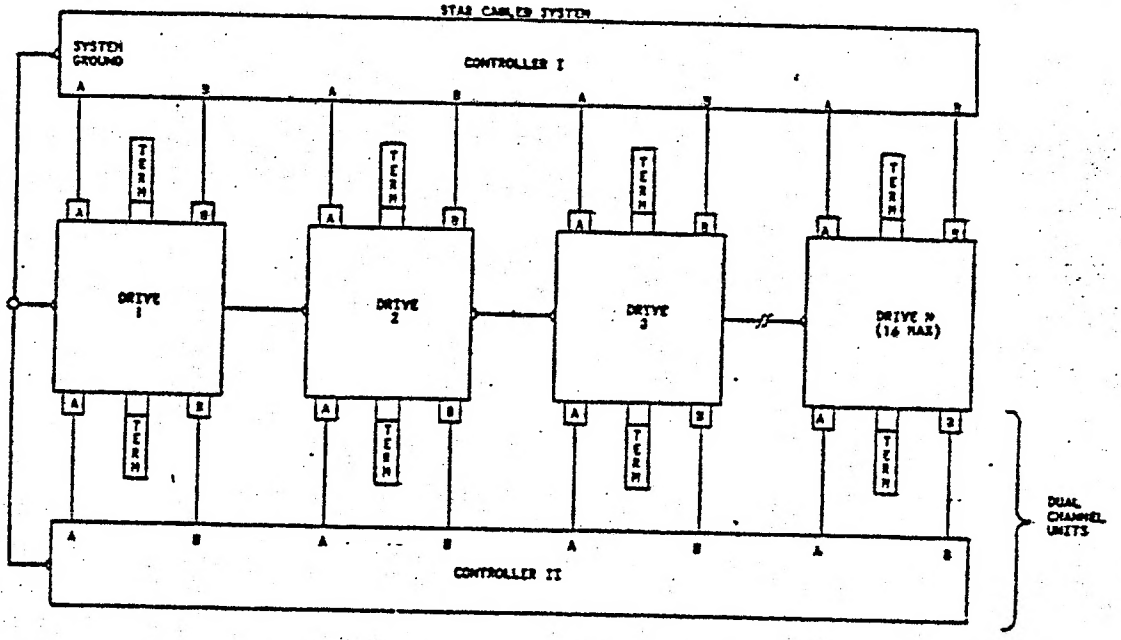
C115A

J1 A Cable Input
J2 A Cable Outrut (or terminator)
J3 B Cable

J1 & J2 are Located on the I/O PWA.

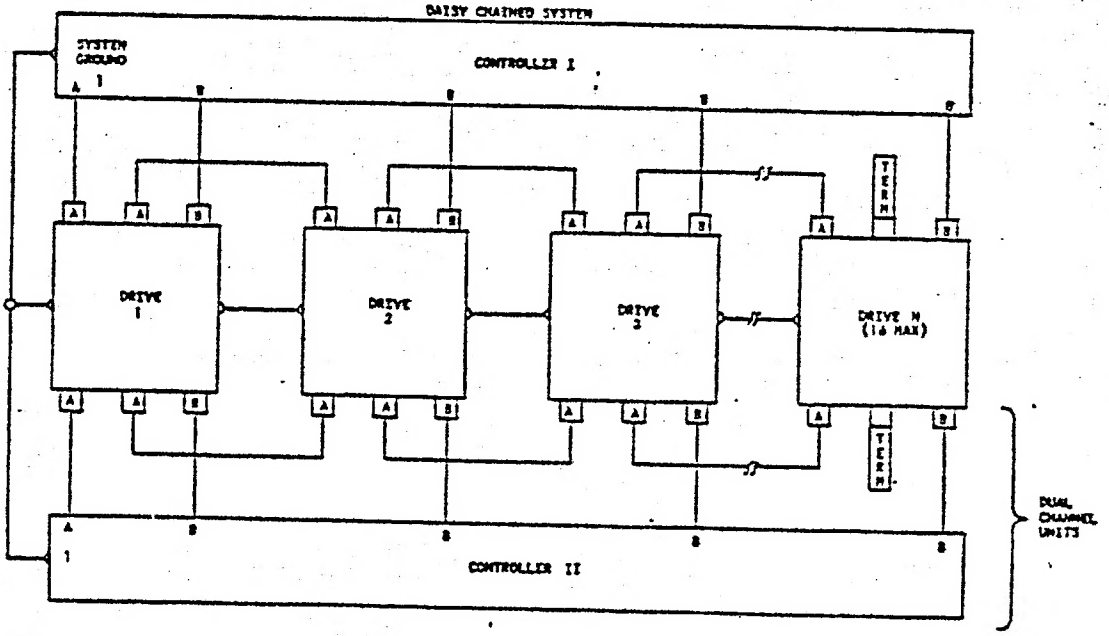
J3 is Located on the CTR/MUX PWA.

FIGURE 15D. I/O CONNECTORS - CMD



NOTES

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET



NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR. SEE 6.1.4.1. 81670
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND AT ONE OF THE UNIT'S RECEIVER CARDS. SEE 6.1.4.2.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 180 FEET.
   MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET.

FIGURE 16. UNIT CABLING

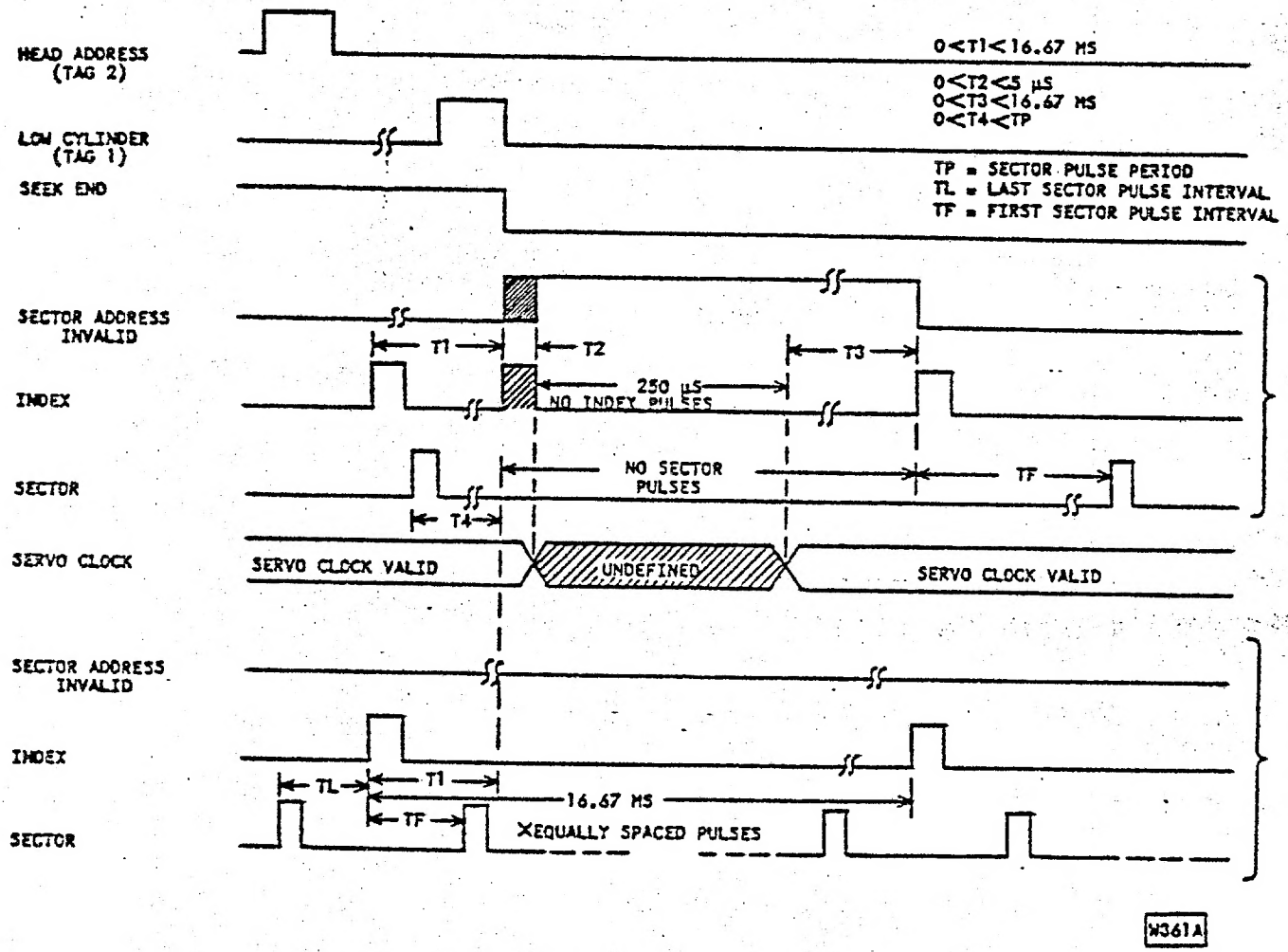


FIGURE 17. INDEX AND SECTOR PULSES DURING SEEK - CMD